

# GA-MA790FX-DQ6

Revision : 1.0

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## SHEET TITLE

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GIGABYTE CORP.

BLOCK DIAGRAM		
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**Model Name:GA-MA790FX-DQ6**

### Component value change history

[illegible]

### Circuit or PCB layout change for next version

[illegible]

## HAMMERHEAD CUSTOMER DESKTOP REFERENCE DESIGN



Title			
<b>BLOCK DIAGRAM</b>			
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L0\_CADIN\_L[0..15] <L0\_CADIN\_L[0..15] [11]  
L0\_CADIN\_H[0..15] <L0\_CADIN\_H[0..15] [11]  
L0\_CLKIN\_L[0..1] <L0\_CLKIN\_L[0..1] [11]  
L0\_CLKIN\_H[0..1] <L0\_CLKIN\_H[0..1] [11]  
L0\_CADOUT\_L[0..15] <L0\_CADOUT\_L[0..15] [11]  
L0\_CADOUT\_H[0..15] <L0\_CADOUT\_H[0..15] [11]  
L0\_CLKOUT\_L[0..1] <L0\_CLKOUT\_L[0..1] [11]  
L0\_CLKOUT\_H[0..1] <L0\_CLKOUT\_H[0..1] [11]

CPU\_VDD\_RUN = VCORE  
CPU\_VDDA\_RUN = VDDA25  
VLDT\_RUN = VCC12\_HT  
CPU\_VDDIO\_SUS = DDR18V  
CPU\_VTT\_SUS = DDRVTT

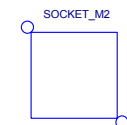
VLDT\_A = VCC12\_HT  
VLDT\_B = HT12B



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CPU-SK/940AM2/S/15u[10SC1-A01940-11R\_10SC1-A01940-14R]

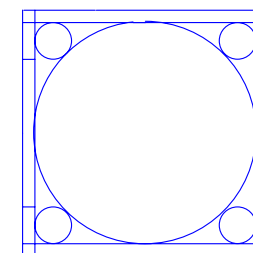
M2 CARZY COOL



CARZY\_COOL[12SP2-060110-01R\_12SP2-060110-02R]

SOCKET\_M2

M2\_RM[12KRC-04K807-31R\_12KRC-04K807-33R]



GIGABYTE CORP.

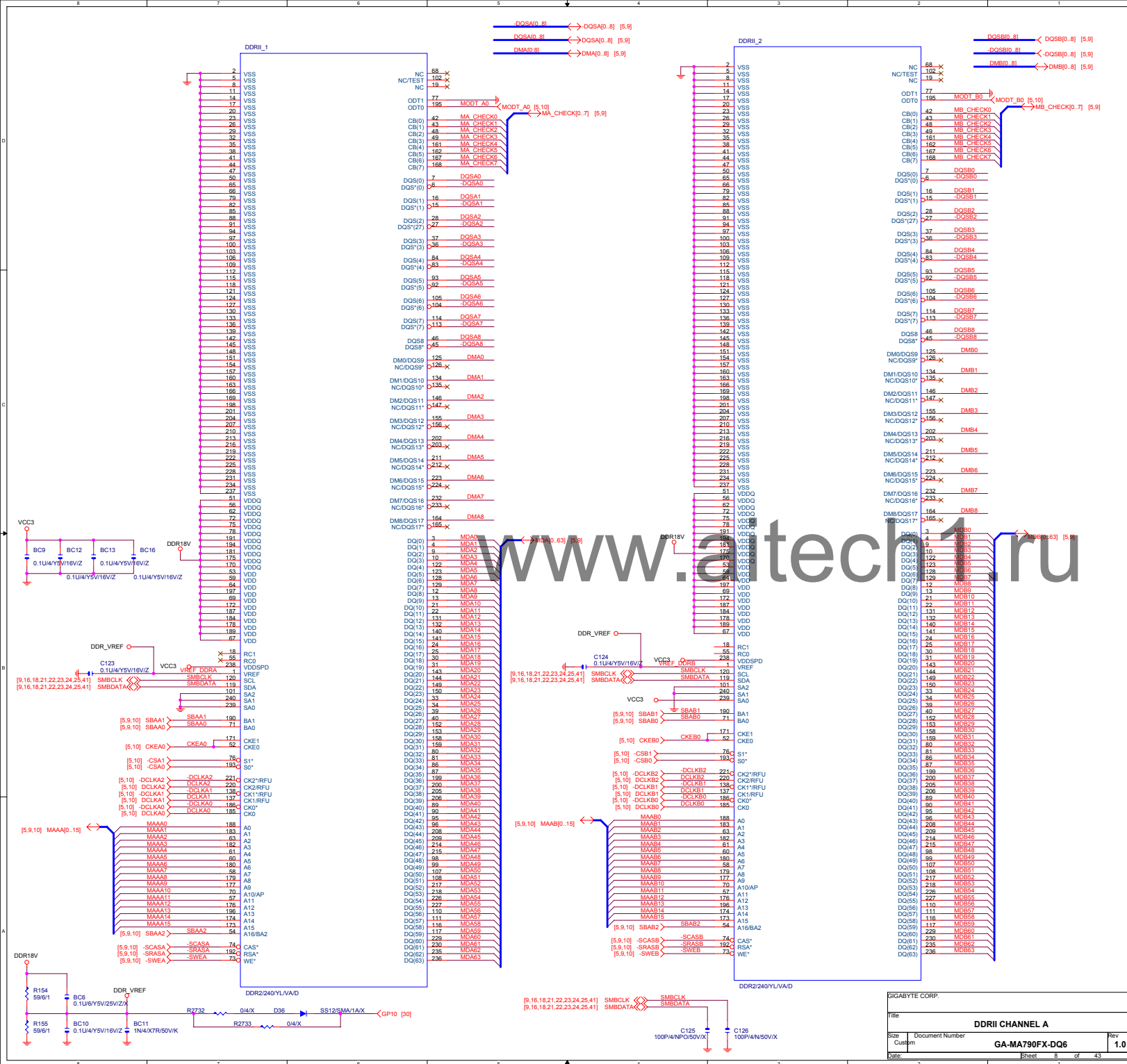
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CPU HYPER TRANSPORT			
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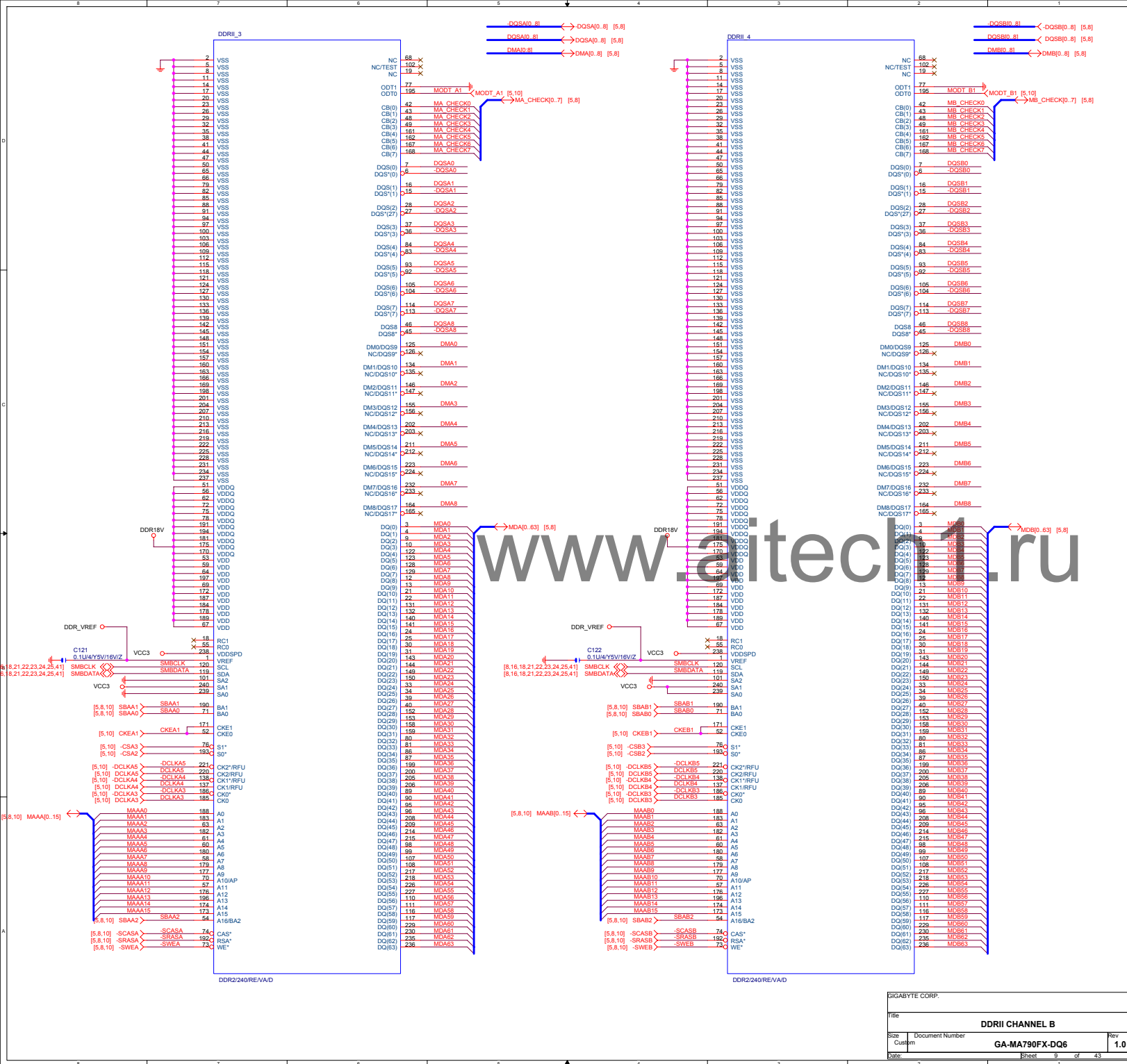




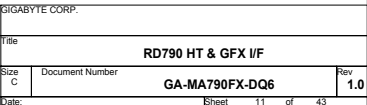


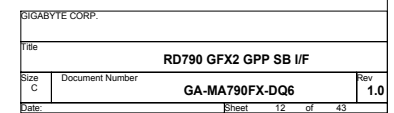


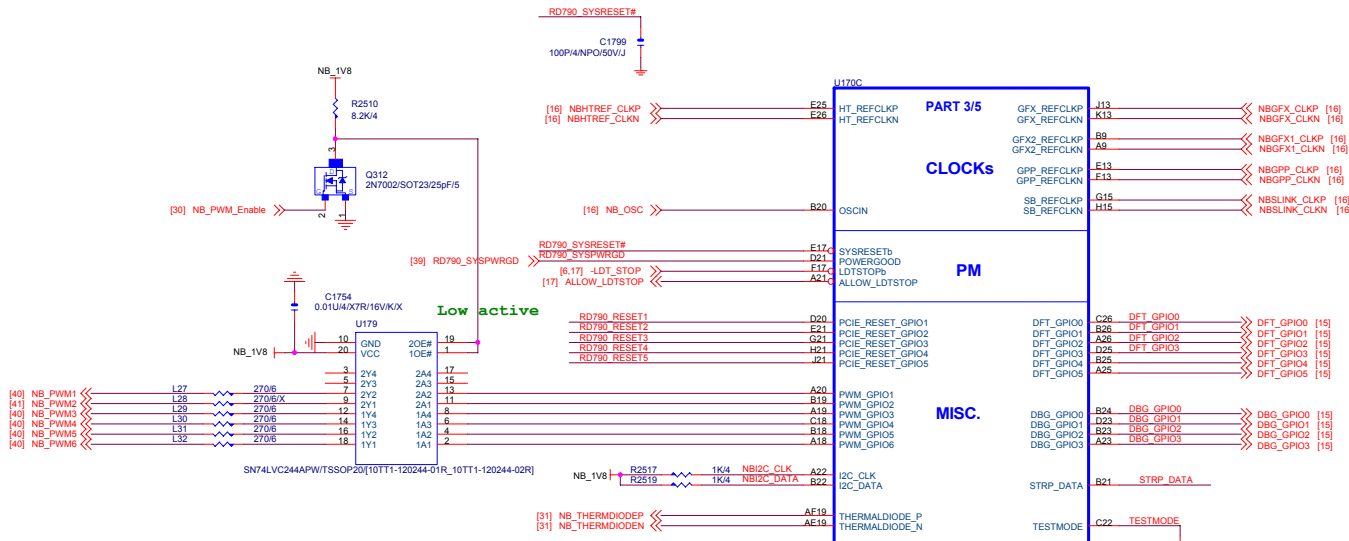




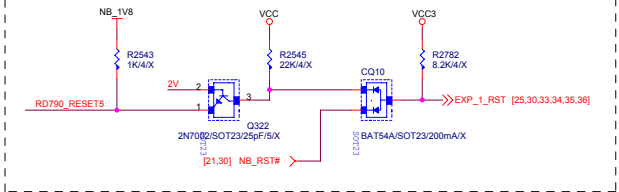
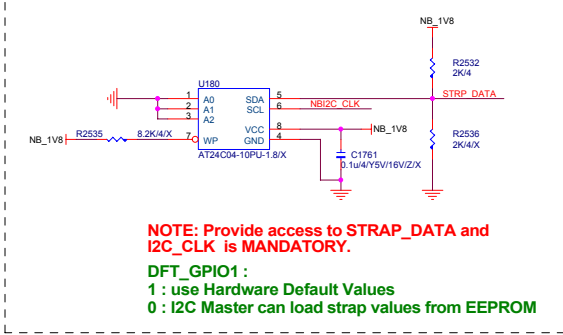
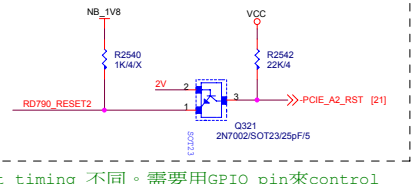
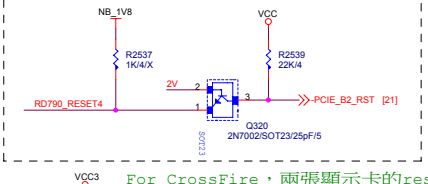
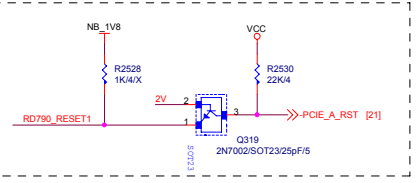
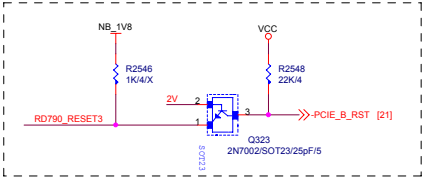
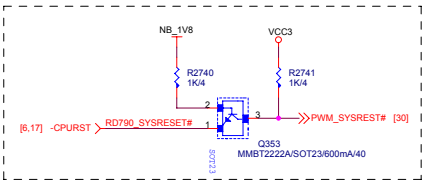








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[13] DFT\_GPIO5 << R2391 1K/4/X

#### DFT\_GPIO5: STRAP\_DEBUG\_BUS\_GPIO\_ENABLED

Enables the Test Debug Bus using GPIO.  
1 : Disable ( Can still be enabled using nbcfg register access)  
0 : Enable

[13] DFT\_GPIO4 << R2392 1K/4

[13] DFT\_GPIO3 << R2393 1K/4/X

[13] DFT\_GPIO2 << R2394 1K/4

#### DFT\_GPIO[4:2]: STRAP\_PCIE\_GPP\_CFG[2:0]

These pin straps are used to configure PCI-E GPP mode.  
(GPIO4 , GPIO3 , GPIO2 )  
000 : 00001 ( 4 + 2 )  
001 : 00010 ( 4 + 1 + 1 )  
010 : 01011 ( 1 + 1 + 1 + 1 + 1 + 1 )  
011 : 00100 ( 2 + 1 + 1 + 1 + 1 )  
100 : 01010 ( 2 + 2 + 1 + 1 )  
101 : 01100 ( 2 + 2 + 2 )  
111 : 01011 ( 1 + 1 + 1 + 1 + 1 + 1 ) or EEPROM

[13] DFT\_GPIO1 << R2395 1K/4/X

#### DFT\_GPIO1: LOAD\_EEPROM\_STRAPS

Selects Loading of STRAPS from EPROM  
1 : Bypass the loading of EEPROM straps and use Hardware Default Values  
0 : I2C Master can load strap values from EEPROM if connected, or use default values if not connected

[13] DFT\_GPIO0 << R2396 1K/4/X

#### DFT\_GPIO0: STRAP\_DEBUG\_BUS\_PCIE\_ENABLED

Enables the Test Debug Bus using PCIE bus  
1 : Disable ( Can still be enabled using nbcfg register access )  
0 : Enable

[13] DBG\_GPIO0 << 1 TP115

[13] DBG\_GPIO1 << 1 TP116

[13] DBG\_GPIO2 << 1 TP117

[13] DBG\_GPIO3 << 1 TP118

All of the above straps are active low straps and are pulled up internally to work in default states. It is not required to connect any external pull up to these straps. In order to change the default values of the strap, the strap pins must be pulled down to VSS through a resistor (typically 3 Kohm).

GIGABYTE CORP.

Title

**RD790 STRAPS**

Size  
B

Document Number

**GA-MA790FX-DQ6**

Rev  
**1.0**

Date:

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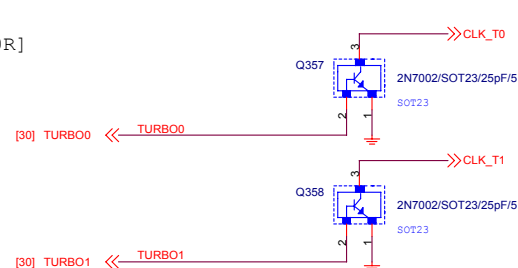
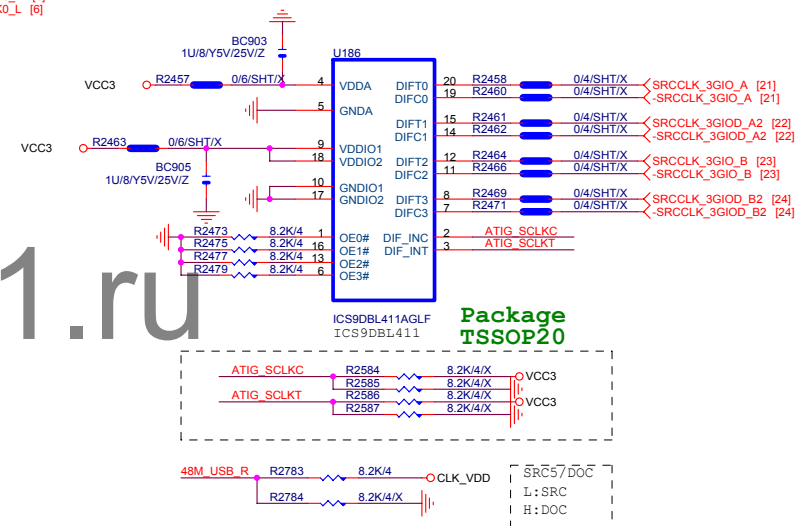
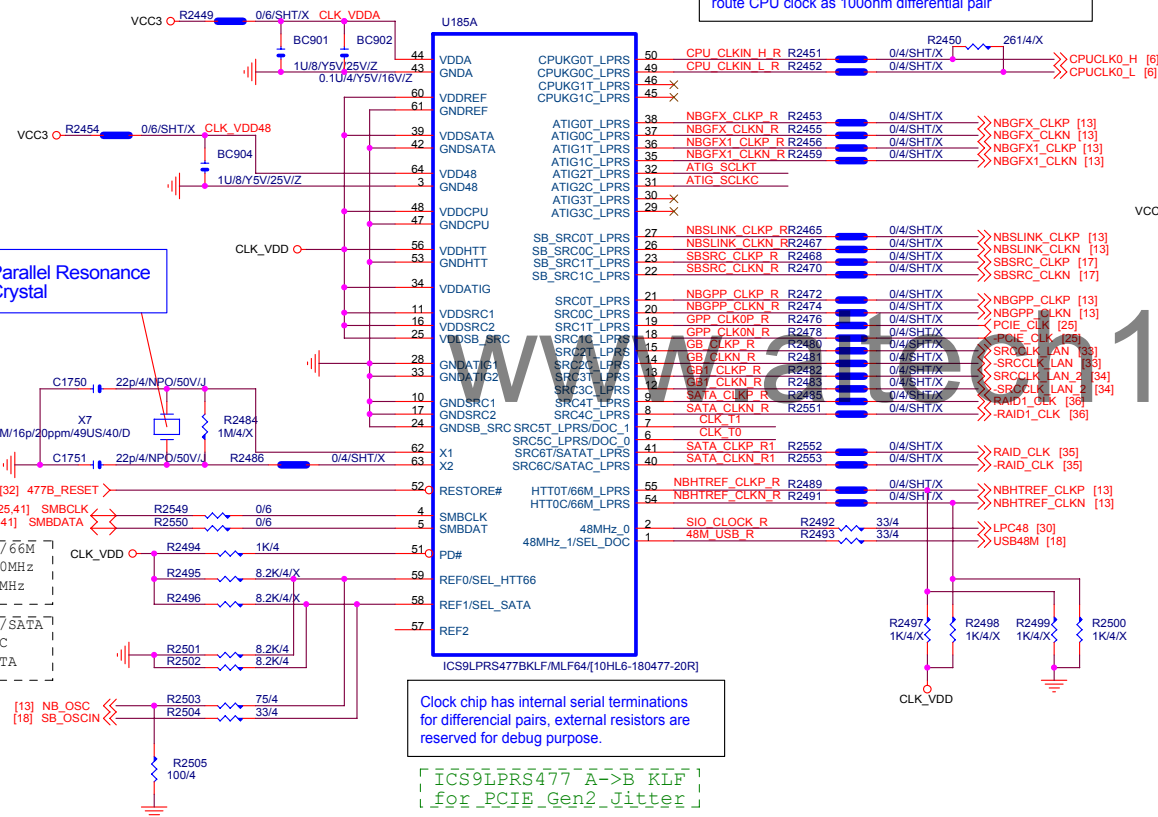


```

1- PLACE ALL THE SERIES TERMINATION
RESISTORS AS CLOSE TO U800 AS
POSSIBLE
2- ROUTE ALL SRCCLKTx AND SRCCLKCx
AS DIFFERENT PAIR RULE
3- PUT DECOUPLING CAPS CLOSE TO U800
POWER PIN

```

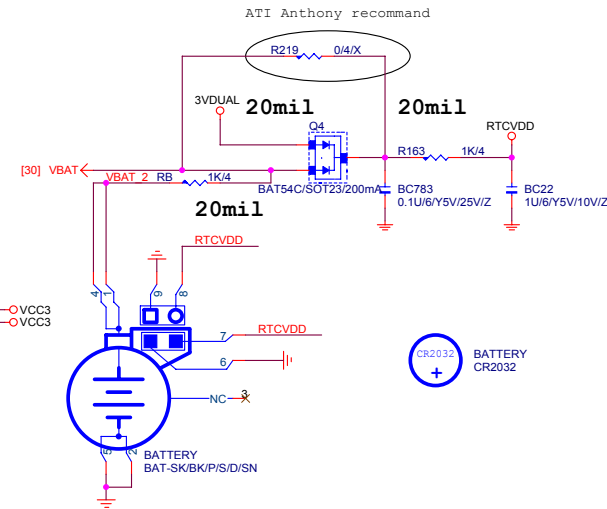
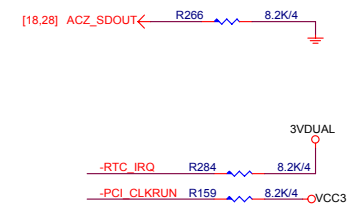
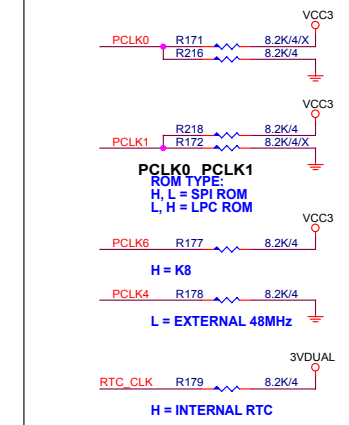
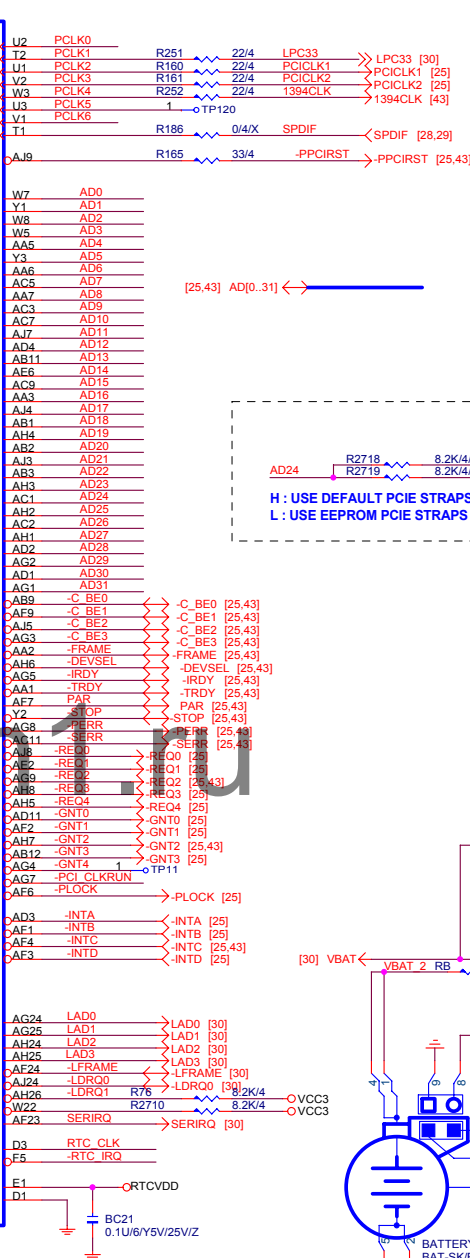
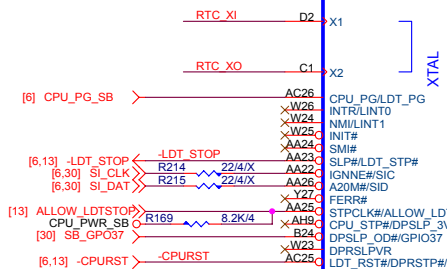
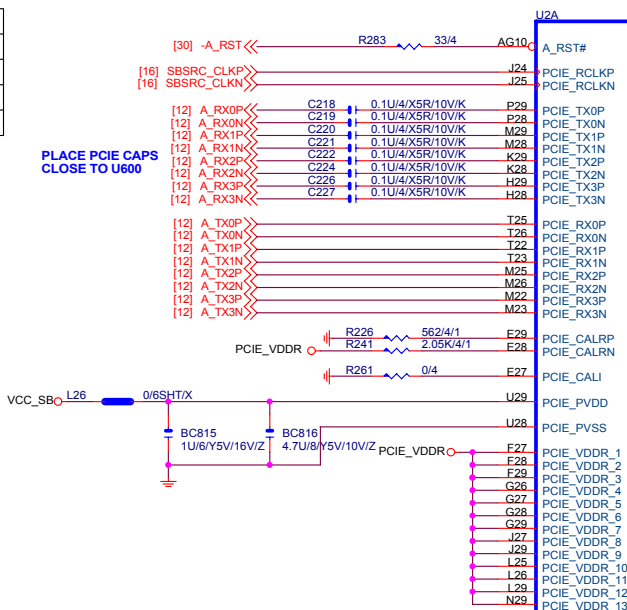
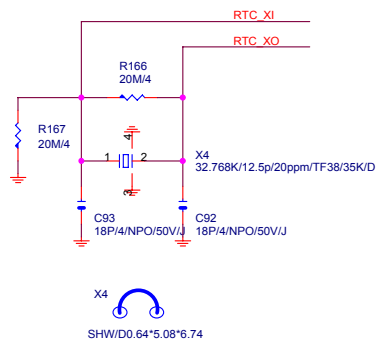
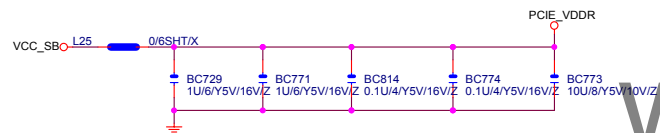
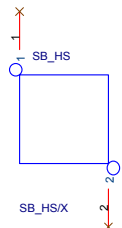
Place R800/801 less than 500 mils away from U800  
R851 less than 100 mils away from R800/801  
route CPU clock as 100ohm differential pair



**GIGABYTE CORP.**

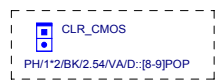
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ICS9LPRS472 , ICS9DBL411			
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**S.B HEATSINK**



CLR_CMOS	
SHORT	CLEAR CMOS
OPEN	NORMAL

**NOT ADD ICT FOR RTCVDD PIN**



**GIGABYTE CORP.**

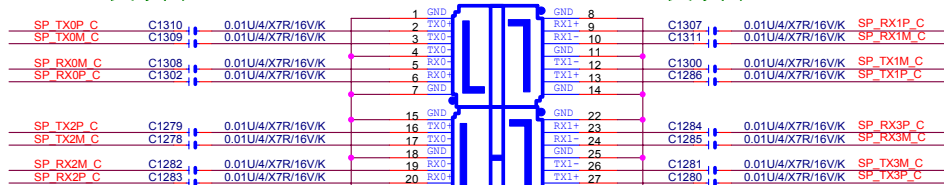
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GA-MA790FX-DQ6

Size Custom	Document Number <b>GA-MA790FX-DQ6</b>	Rev <b>1</b>
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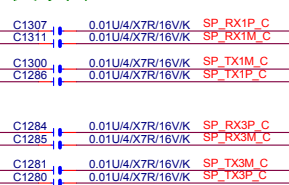
文字面 : SATAII0



文字面 : SATAII1

SATA2/4\*7[11NH5-110228-01R\_11NH5-110228-02R\_11NH5-110228-03R]

文字面 : SATAII2



文字面 : SATAII3



PLACE SATA AC COUPLING  
CAPS CLOSE TO SB600

SB600 SB 23x23mm

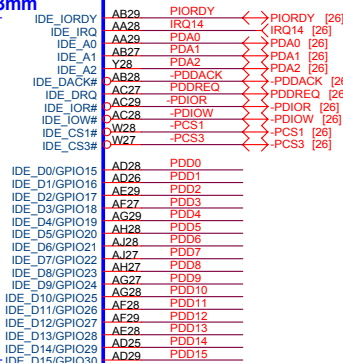
Part 2 of 4

SERIAL ATA

SERIAL ATA POWER

SPIROM

HW MONITOR



PDD[0..15] <--> PDD[0..15] [26]



NOTE: ROUTE TEMP COMM  
AS A 10MIL TRACE

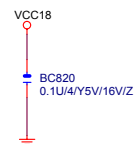
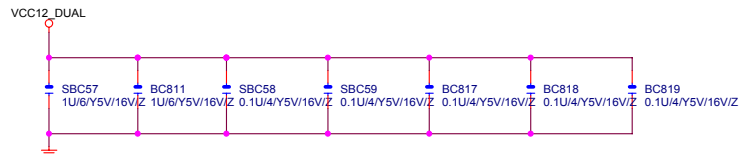
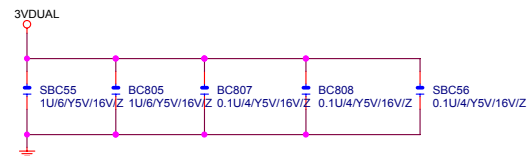
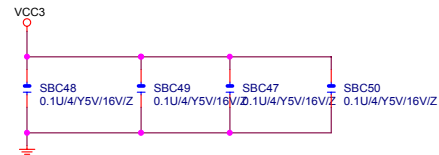
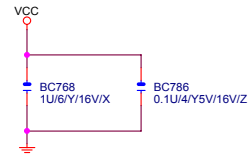
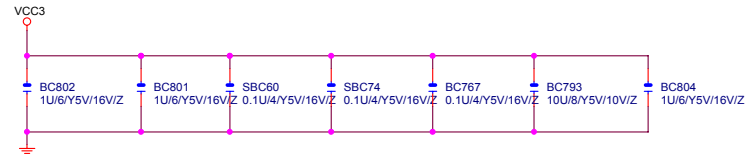
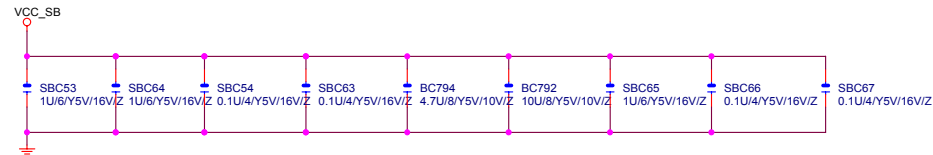


H : LONG RESET  
L : SHORT RESET

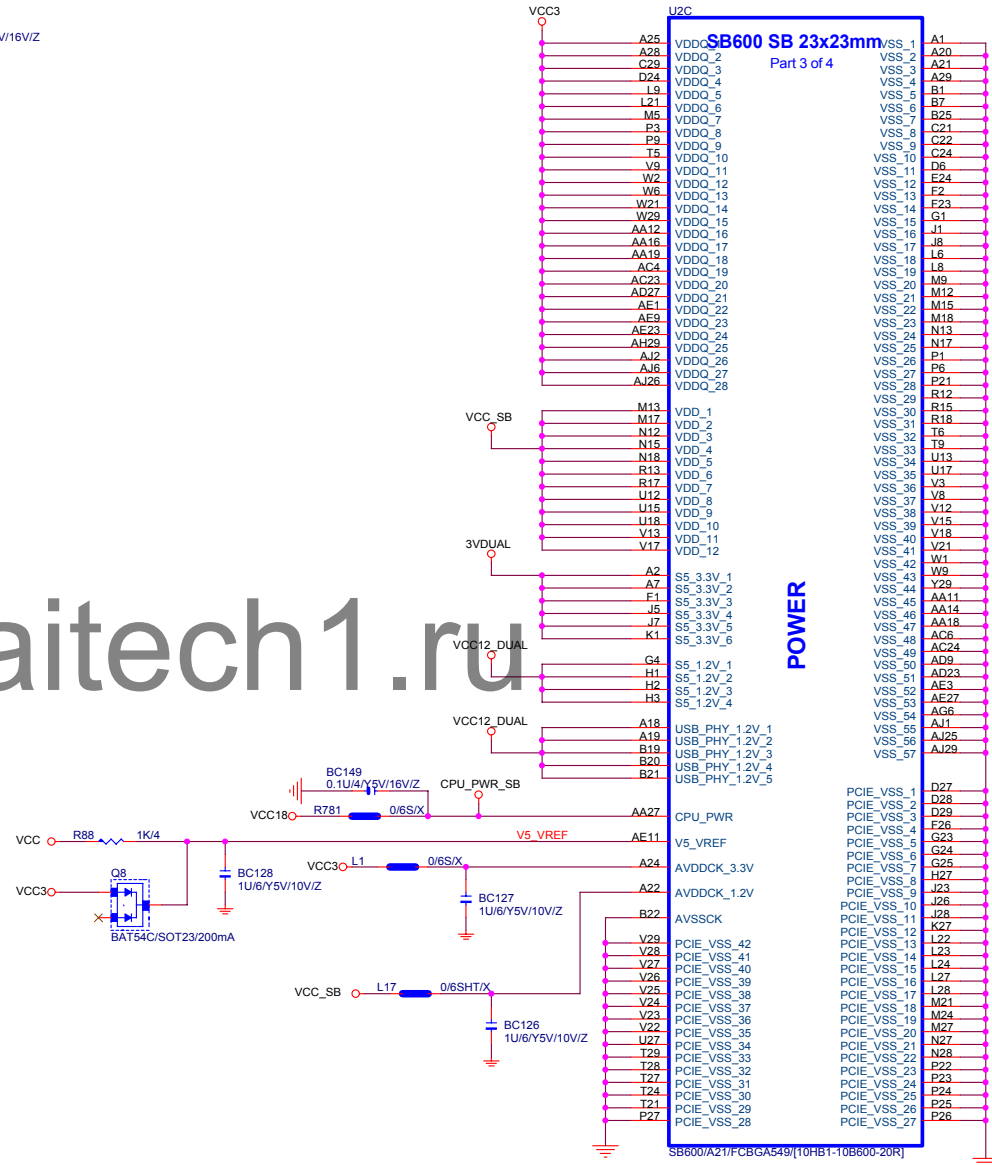
Special NS\_VIA CONNECTS  
HWM\_AGND TO GND at VIA  
hole only

GIGABYTE CORP.

Title			ATI SB600-SATA,PDD,IDE,HWM	
Size	Document Number	GA-MA790FX-DQ6		Rev
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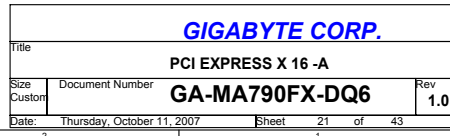


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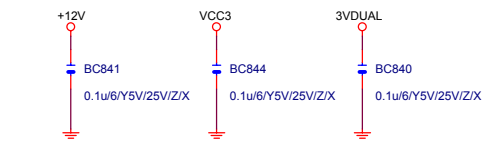
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Size	Document Number	GA-MA790FX-DQ6		Rev
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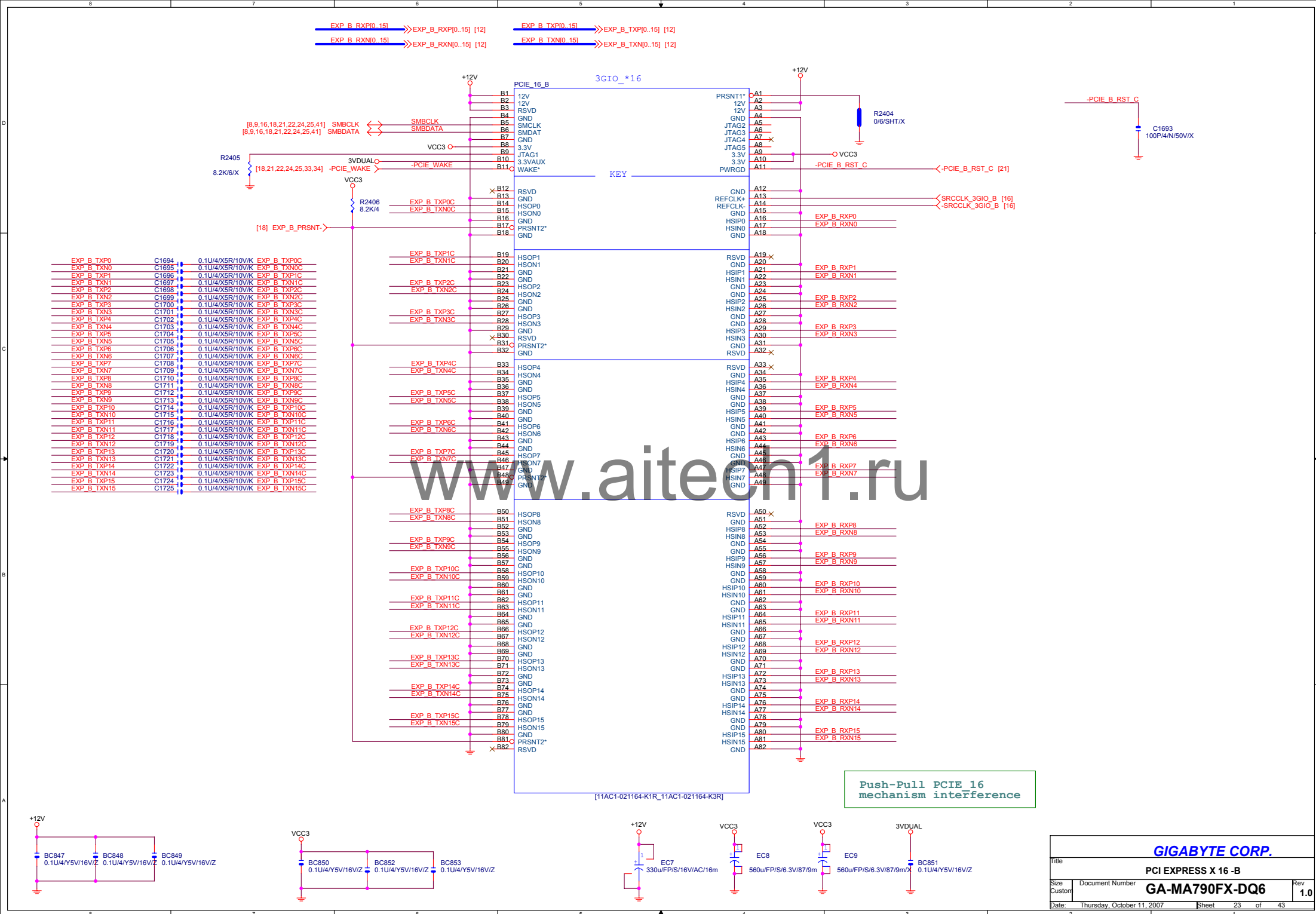


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EXP A2 TXP8	C1677	0.1u4/X5R/10V/K	EXP A2 TXP8C
EXP A2 TXN8	C1678	0.1u4/X5R/10V/K	EXP A2 TXN8C
EXP A2 TXP9	C1679	0.1u4/X5R/10V/K	EXP A2 TXP9C
EXP A2 TXN9	C1680	0.1u4/X5R/10V/K	EXP A2 TXN9C
EXP A2 TXP10	C1681	0.1u4/X5R/10V/K	EXP A2 TXP10C
EXP A2 TXN10	C1682	0.1u4/X5R/10V/K	EXP A2 TXN10C
EXP A2 TXP11	C1683	0.1u4/X5R/10V/K	EXP A2 TXP11C
EXP A2 TXN11	C1684	0.1u4/X5R/10V/K	EXP A2 TXN11C
EXP A2 TXP12	C1685	0.1u4/X5R/10V/K	EXP A2 TXP12C
EXP A2 TXN12	C1686	0.1u4/X5R/10V/K	EXP A2 TXN12C
EXP A2 TXP13	C1687	0.1u4/X5R/10V/K	EXP A2 TXP13C
EXP A2 TXN13	C1688	0.1u4/X5R/10V/K	EXP A2 TXN13C
EXP A2 TXP14	C1689	0.1u4/X5R/10V/K	EXP A2 TXP14C
EXP A2 TXN14	C1690	0.1u4/X5R/10V/K	EXP A2 TXN14C
EXP A2 TXP15	C1691	0.1u4/X5R/10V/K	EXP A2 TXP15C
EXP A2 TXN15	C1692	0.1u4/X5R/10V/K	EXP A2 TXN15C



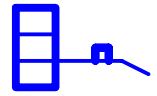




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EXP B2 TXP8	C1727	0.1U/4/X5R/10V/K	EXP B2 TXP8C
EXP B2 TXN8	C1728	0.1U/4/X5R/10V/K	EXP B2 TXN8C
EXP B2 TXP9	C1729	0.1U/4/X5R/10V/K	EXP B2 TXP9C
EXP B2 TXN9	C1730	0.1U/4/X5R/10V/K	EXP B2 TXN9C
EXP B2 TXP10	C1731	0.1U/4/X5R/10V/K	EXP B2 TXP10C
EXP B2 TXN10	C1732	0.1U/4/X5R/10V/K	EXP B2 TXN10C
EXP B2 TXP11	C1733	0.1U/4/X5R/10V/K	EXP B2 TXP11C
EXP B2 TXN11	C1734	0.1U/4/X5R/10V/K	EXP B2 TXN11C
EXP B2 TXP12	C1735	0.1U/4/X5R/10V/K	EXP B2 TXP12C
EXP B2 TXN12	C1736	0.1U/4/X5R/10V/K	EXP B2 TXN12C
EXP B2 TXP13	C1737	0.1U/4/X5R/10V/K	EXP B2 TXP13C
EXP B2 TXN13	C1738	0.1U/4/X5R/10V/K	EXP B2 TXN13C
EXP B2 TXP14	C1739	0.1U/4/X5R/10V/K	EXP B2 TXP14C
EXP B2 TXN14	C1740	0.1U/4/X5R/10V/K	EXP B2 TXN14C
EXP B2 TXP15	C1741	0.1U/4/X5R/10V/K	EXP B2 TXP15C
EXP B2 TXN15	C1742	0.1U/4/X5R/10V/K	EXP B2 TXN15C

PCIE\_8\_B1



PCIE\_8[12(KRC-080002-02R)]X

+12V

BC855

0.1u/6/Y5V/25V/Z/X

VCC3

BC858

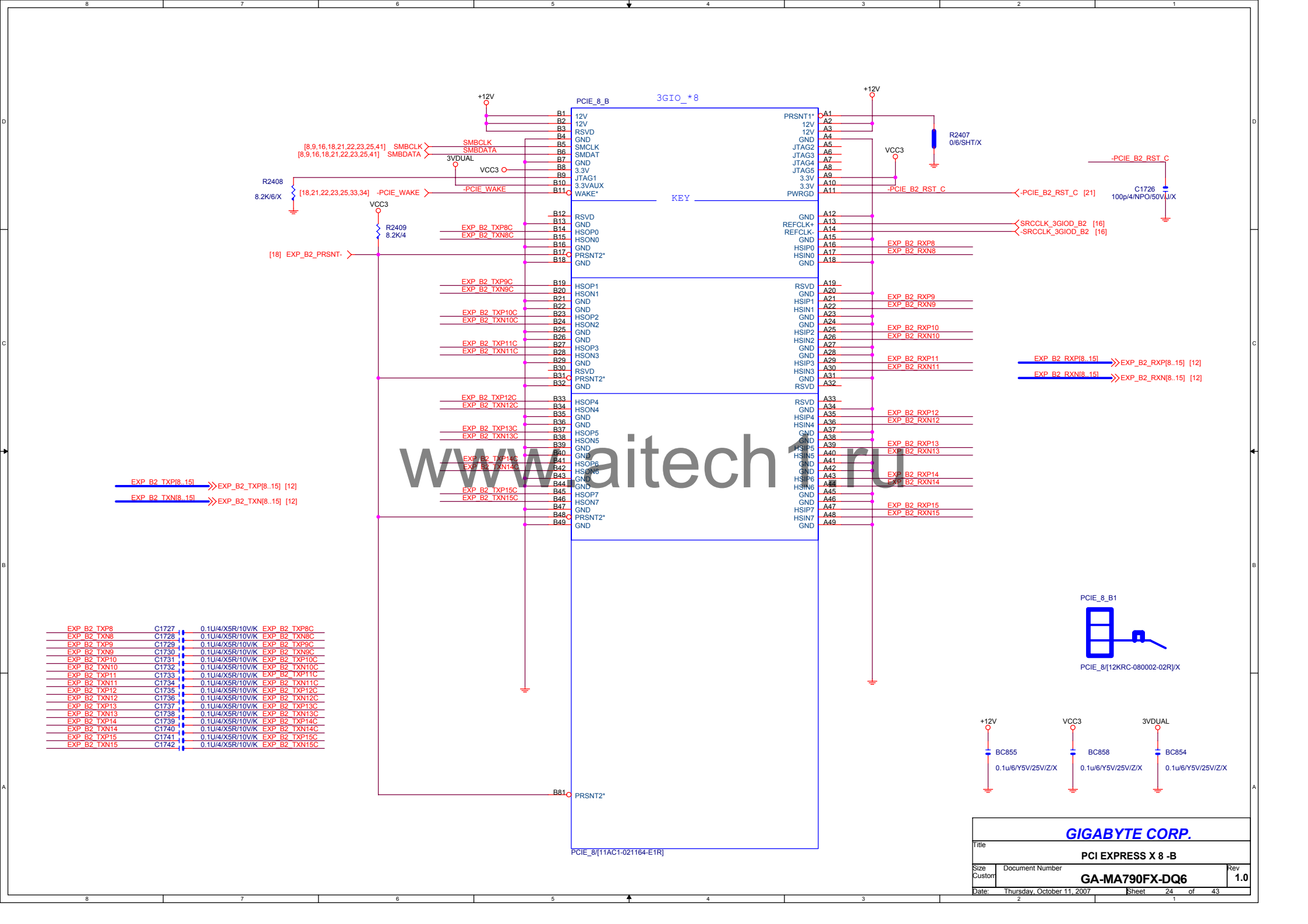
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3VDUAL

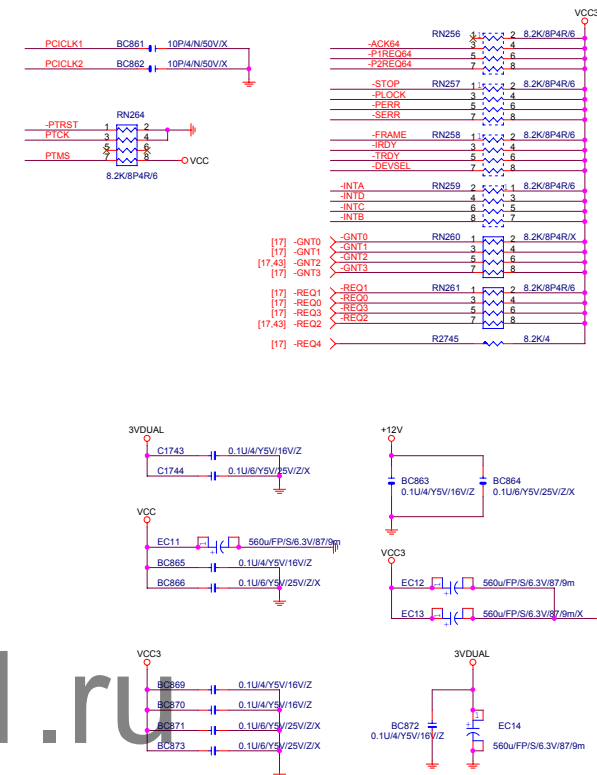
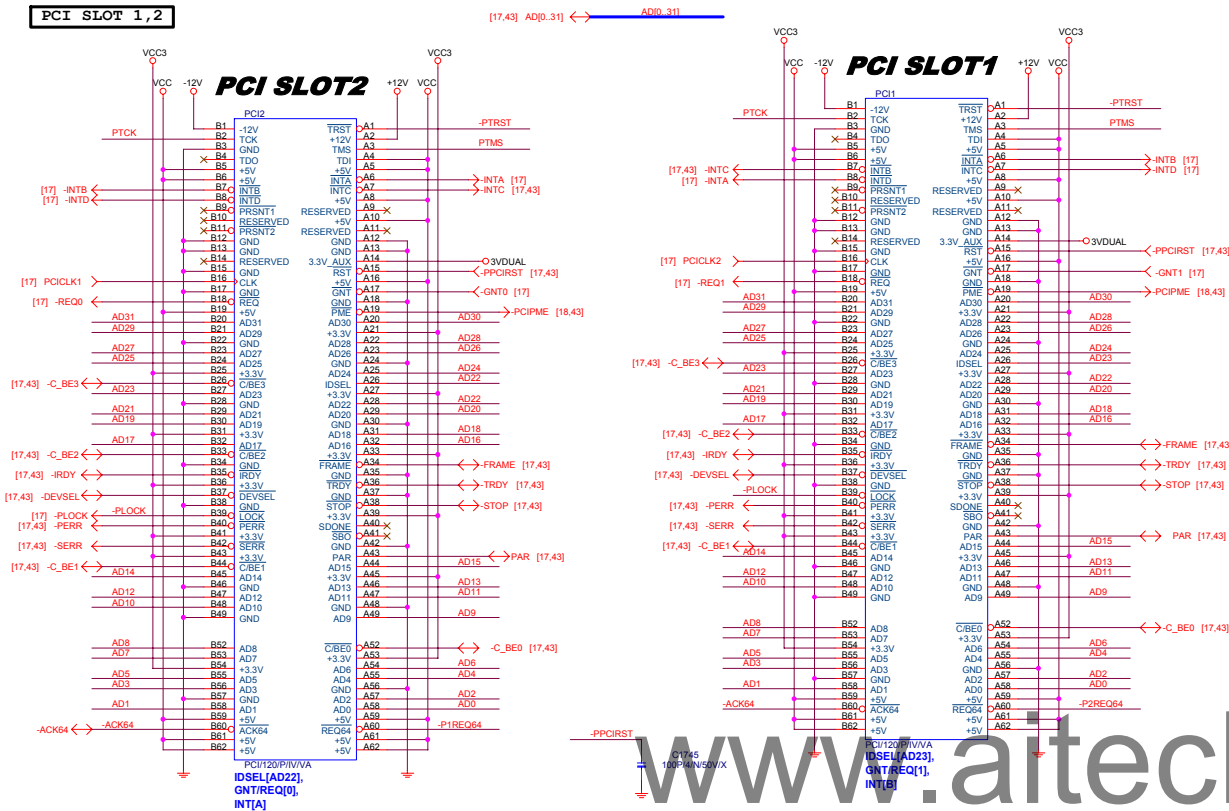
BC854

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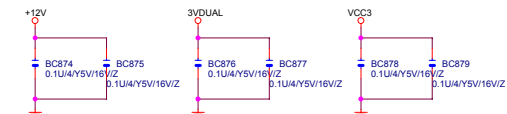
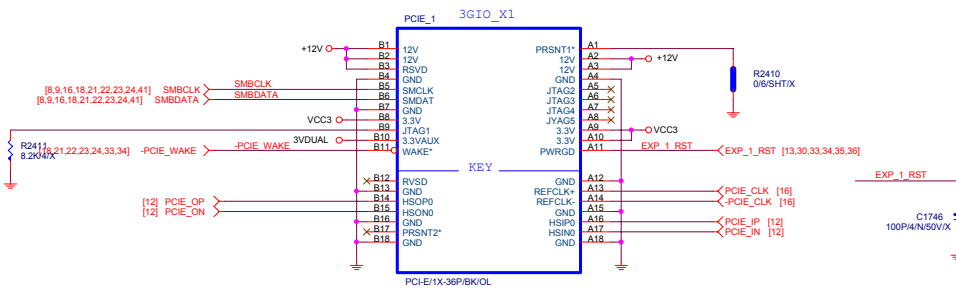
GIGABYTE CORP.		
Title		
PCI EXPRESS X 8 -B		
Size	Document Number	Rev
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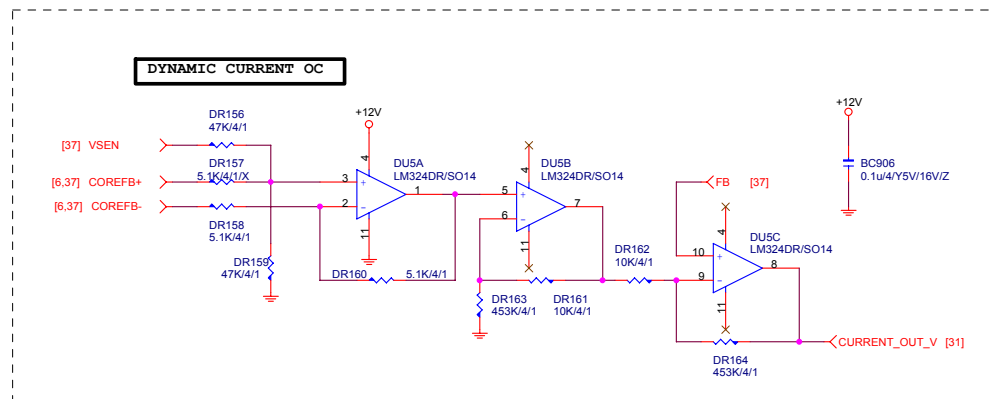
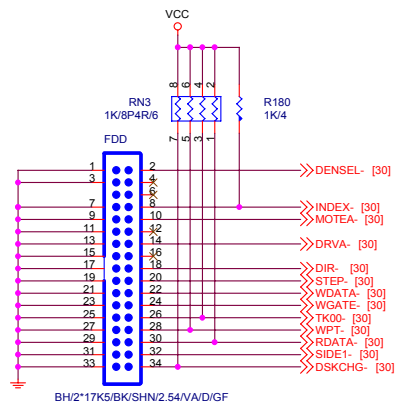


PCI SLOT 1,2
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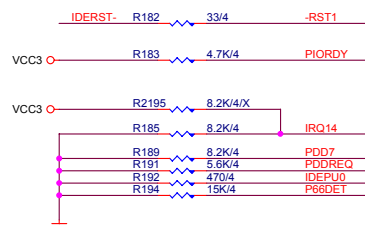


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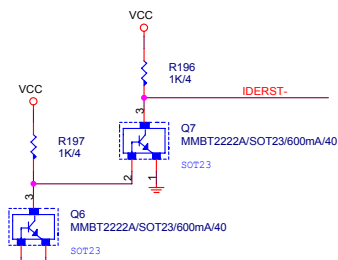
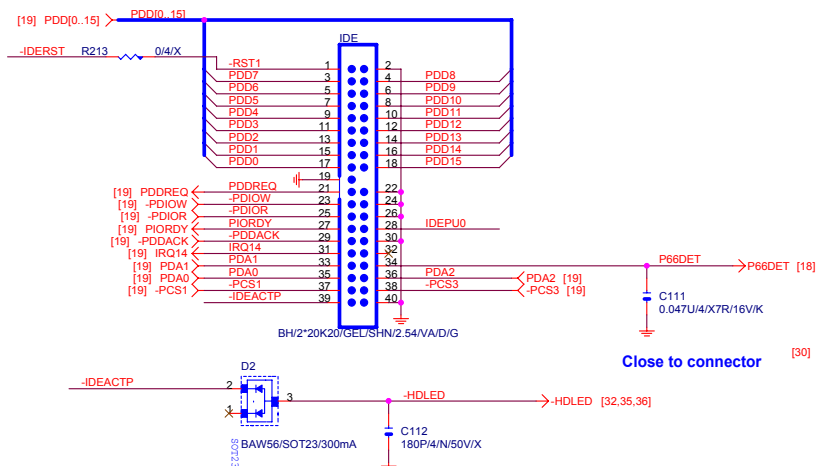




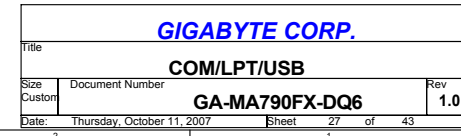
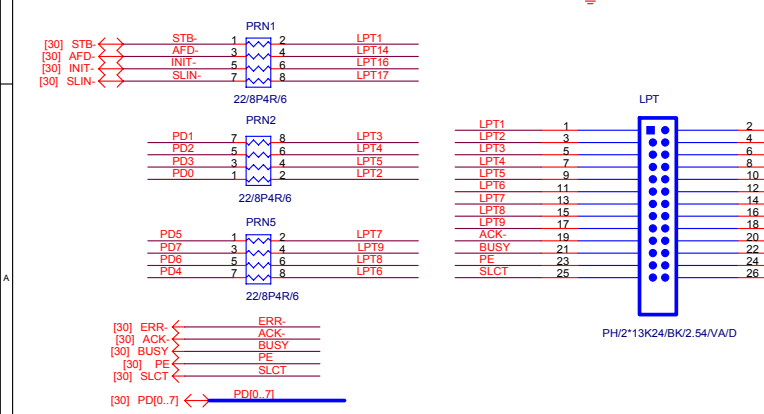
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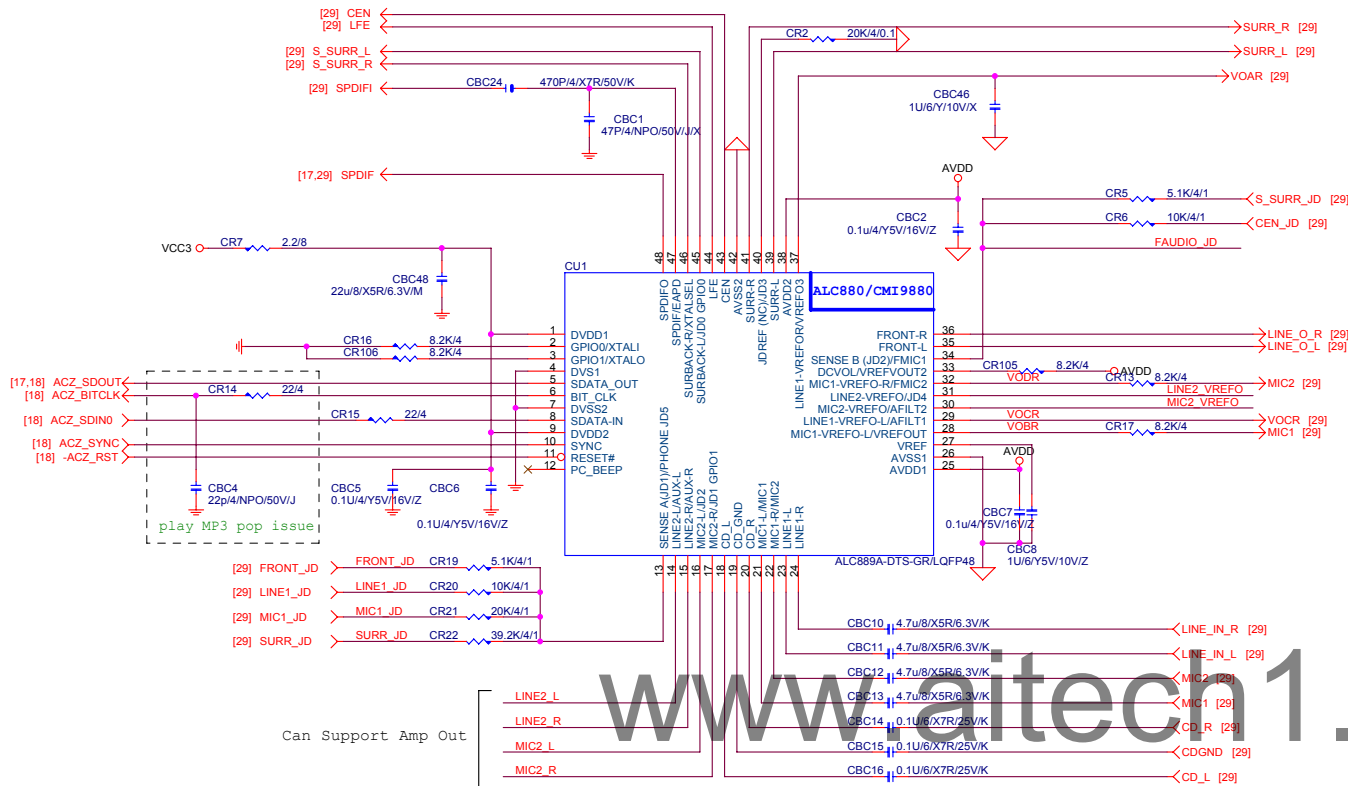


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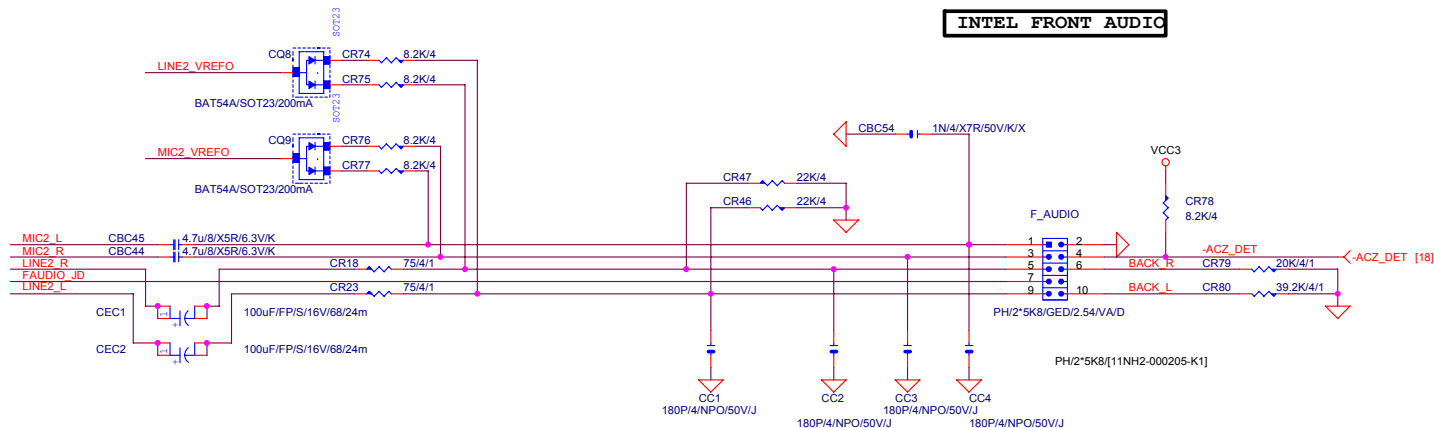


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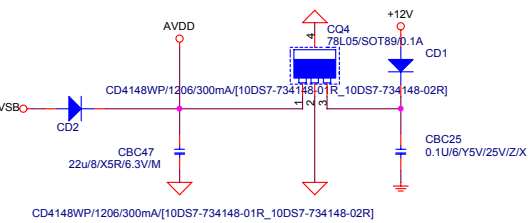
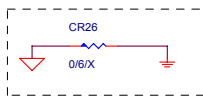


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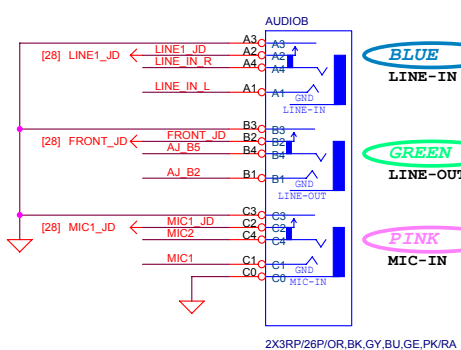
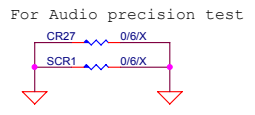
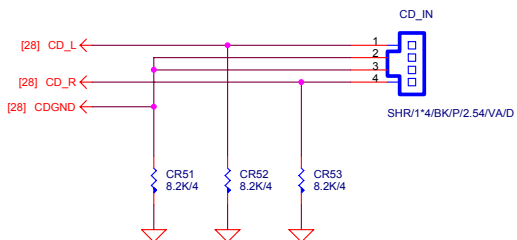


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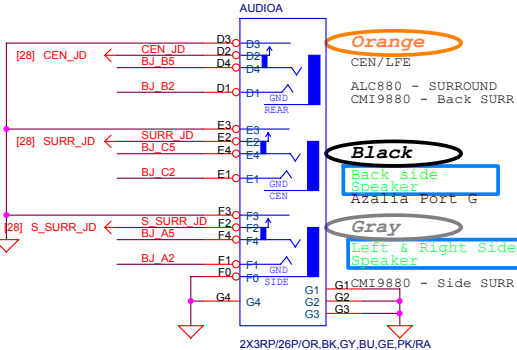
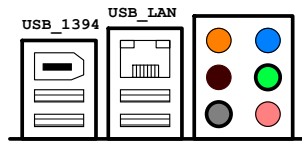
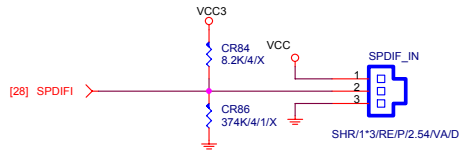
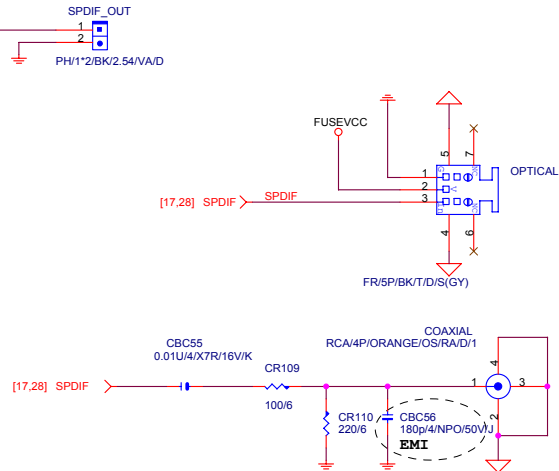
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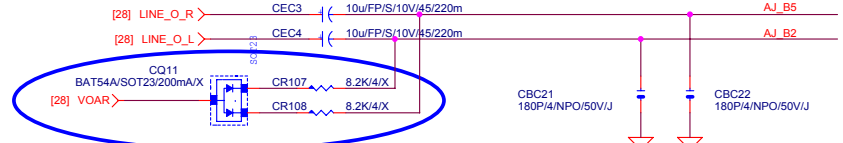


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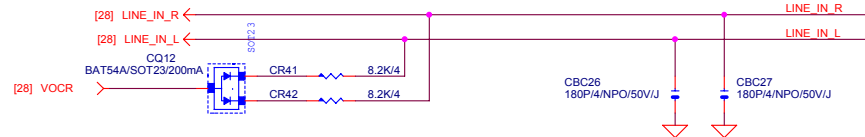


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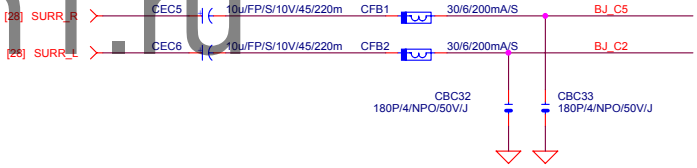
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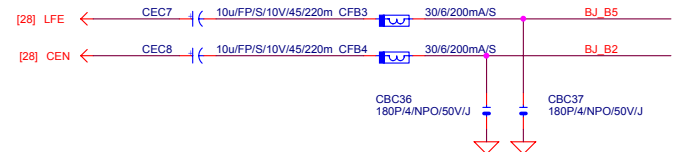
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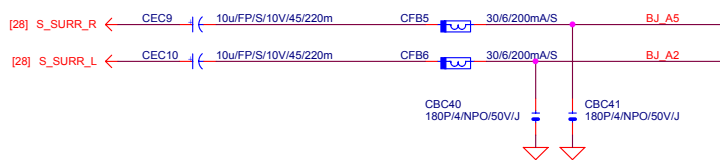
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### CEN/LFE



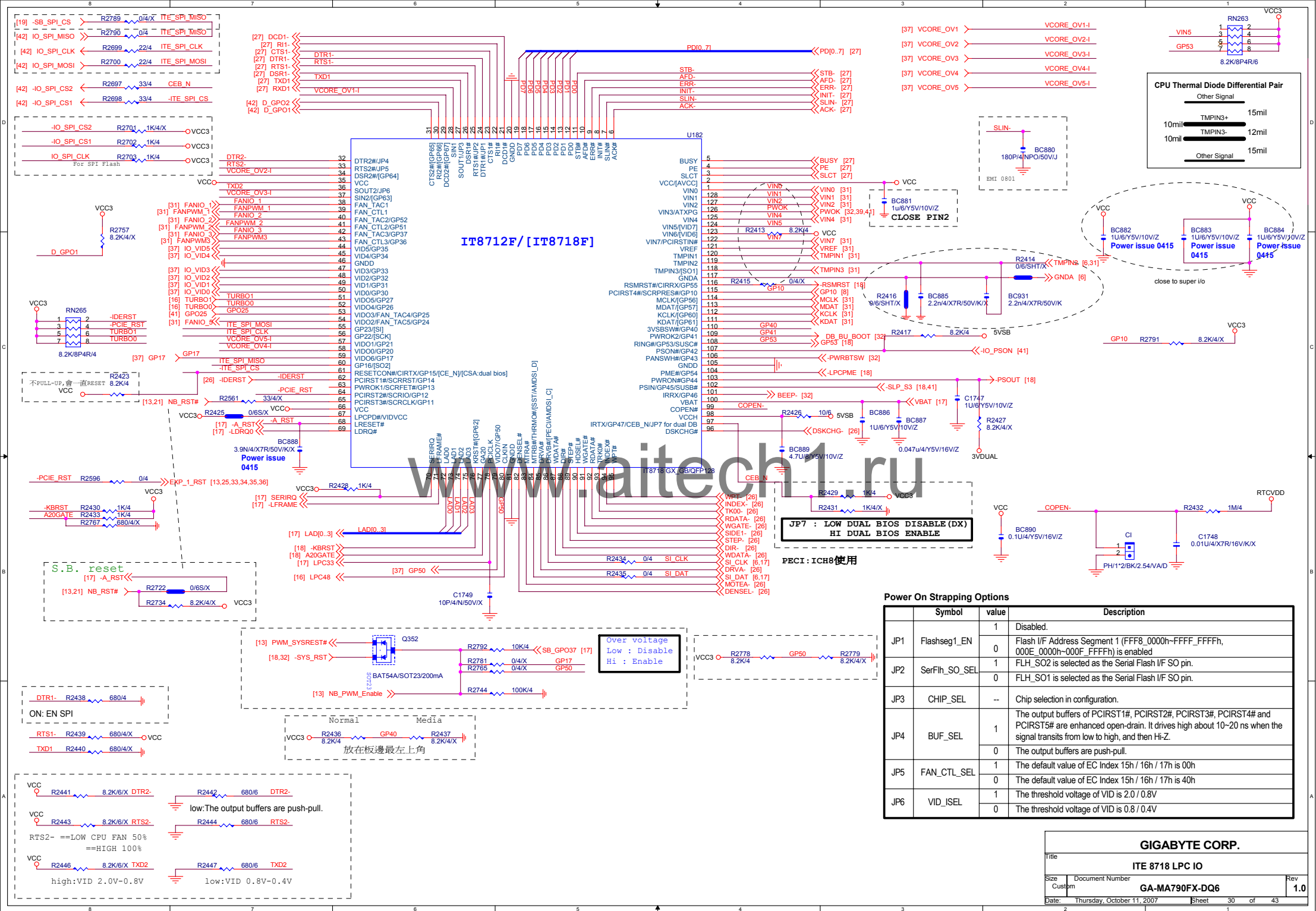
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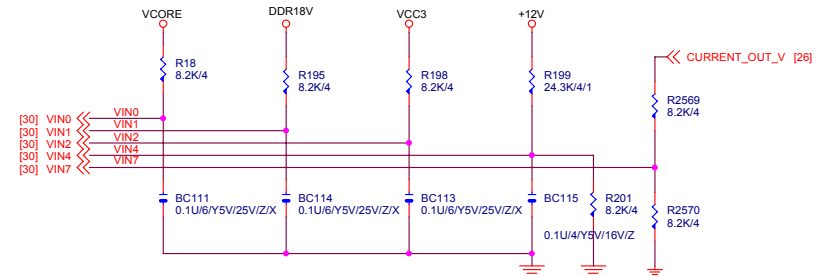
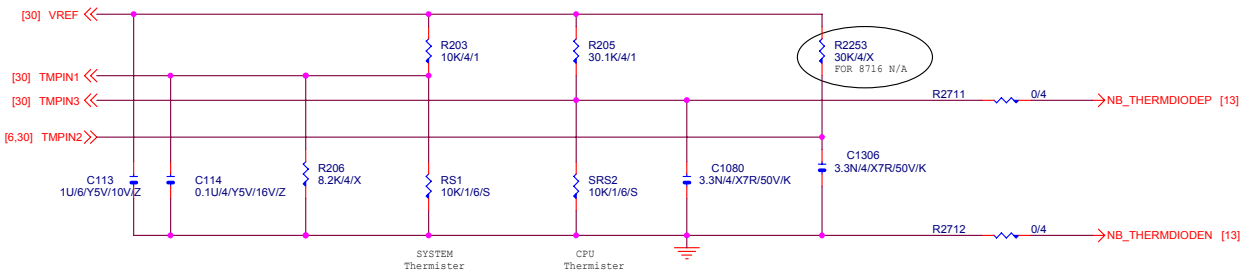
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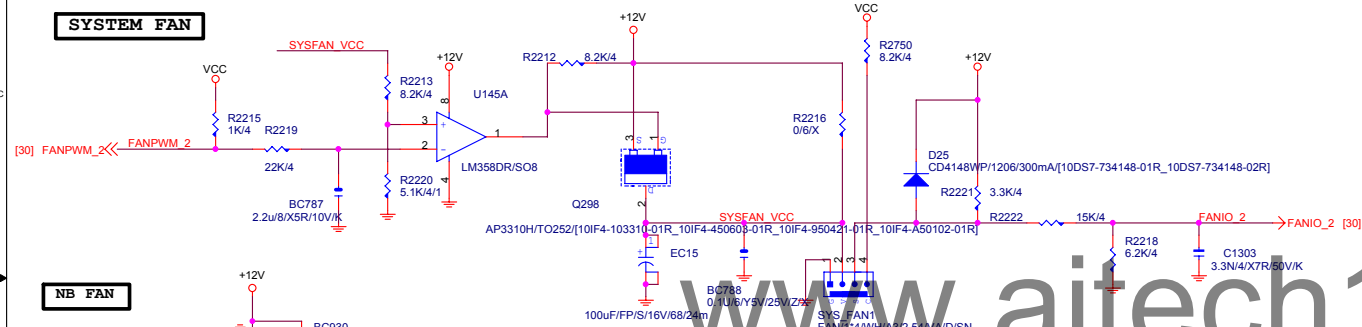




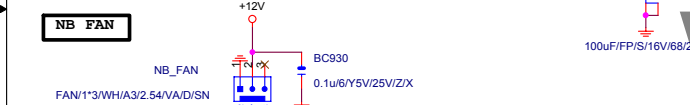
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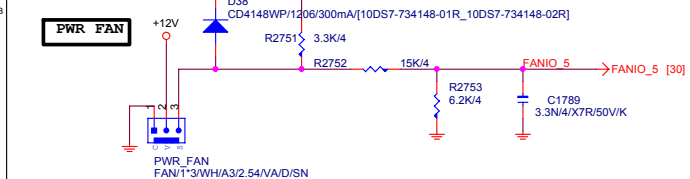
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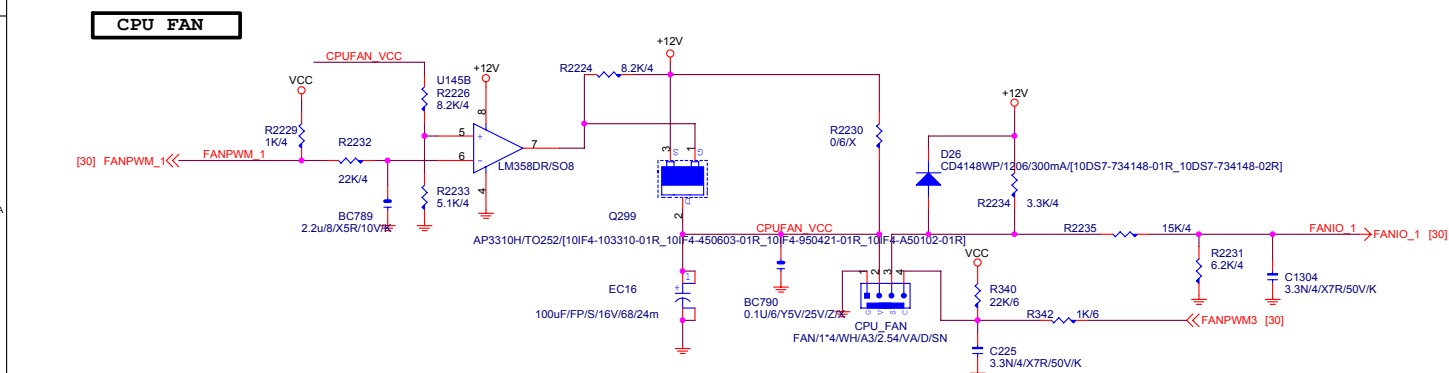
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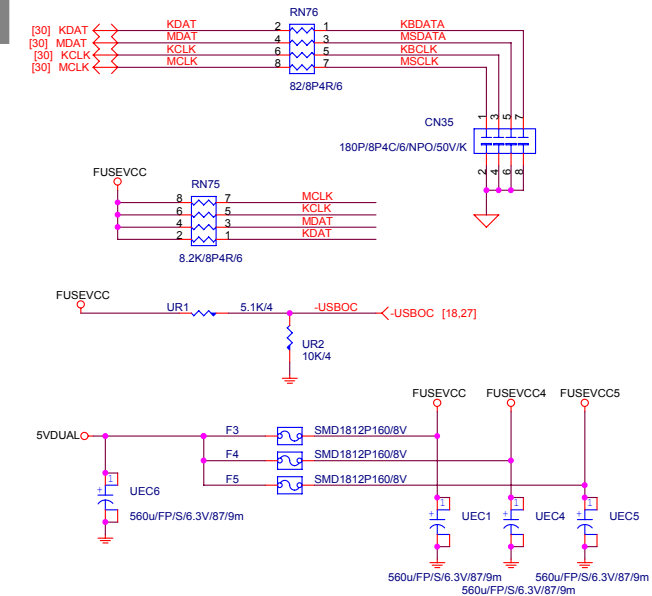
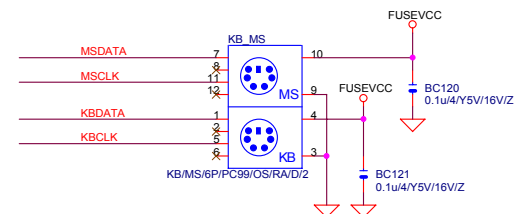
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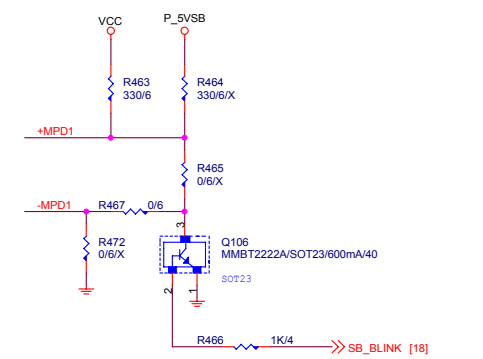
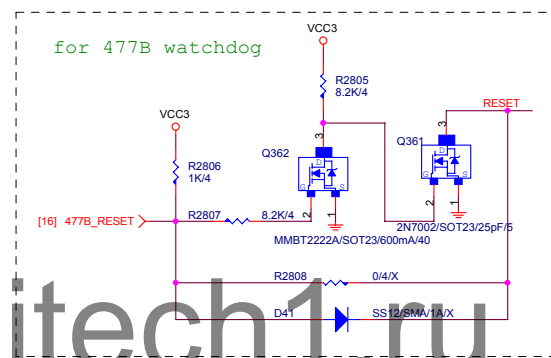
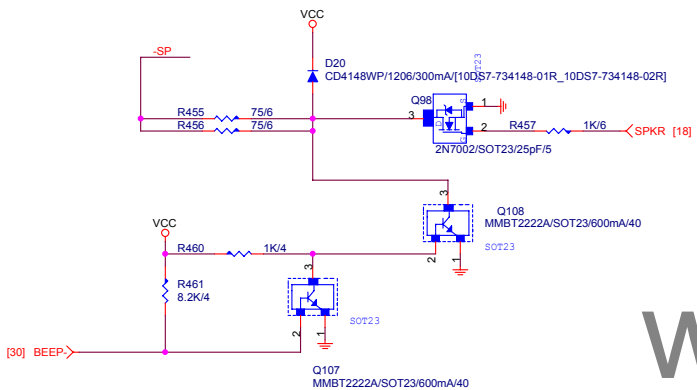
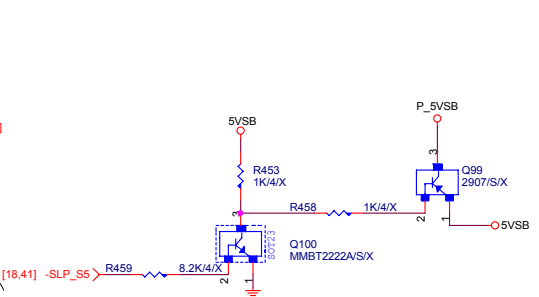
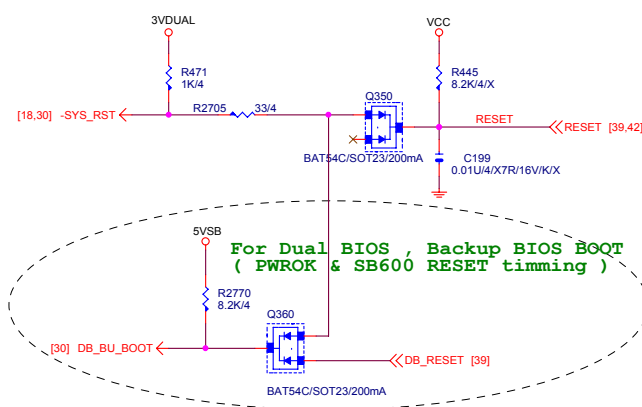
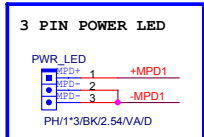
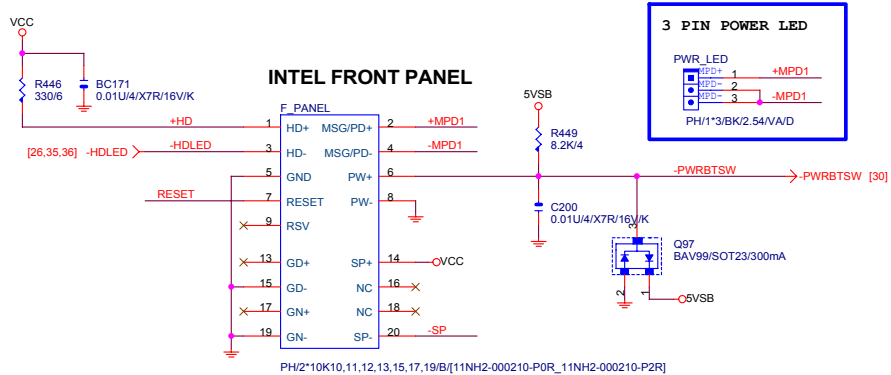


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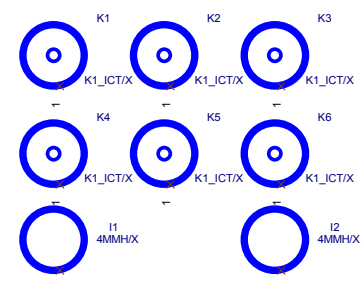
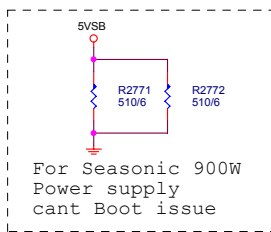
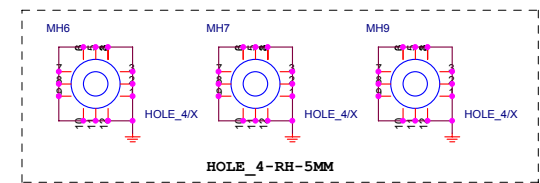
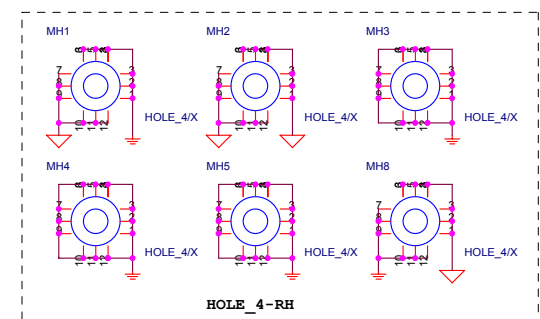
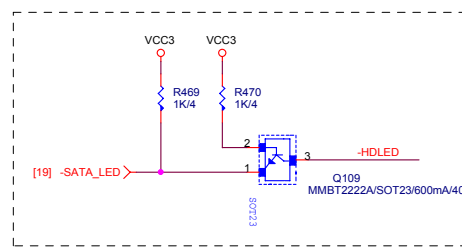
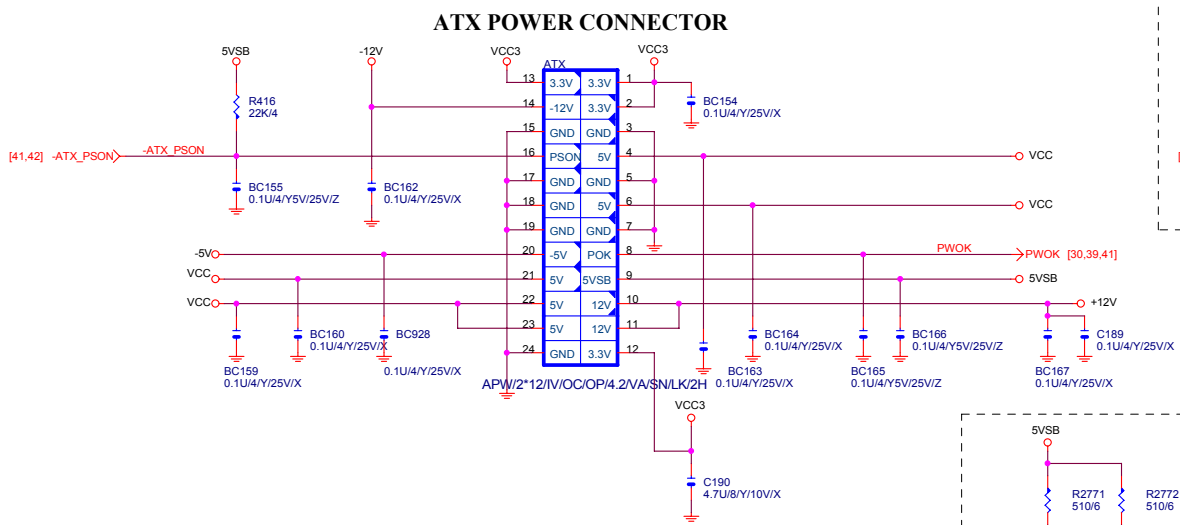


**KB & MS**



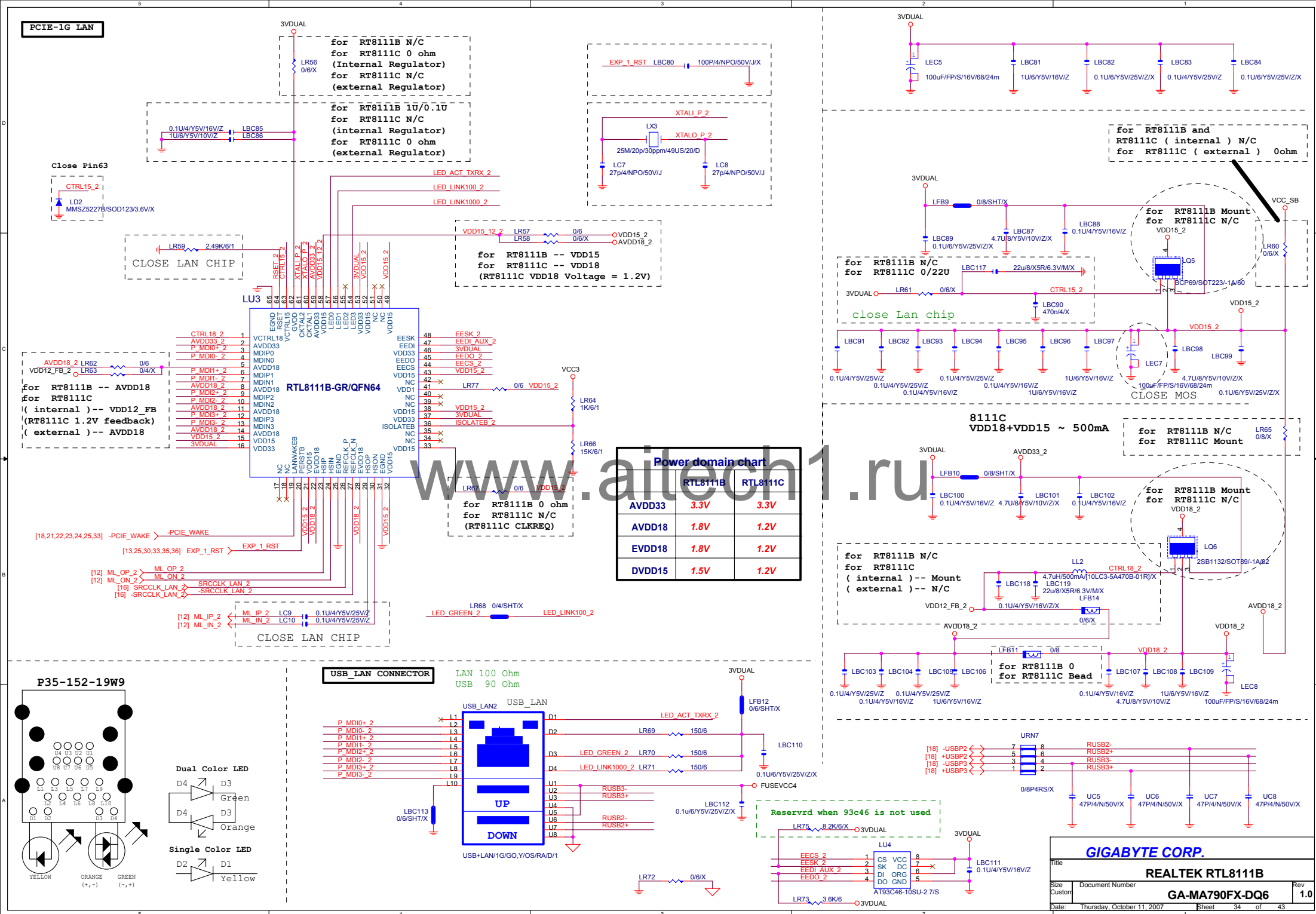


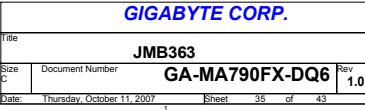
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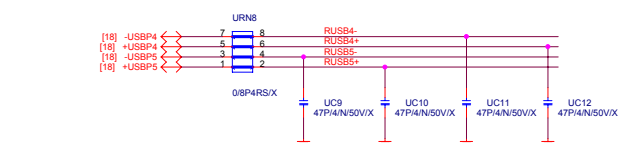
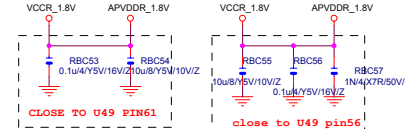
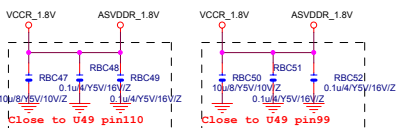
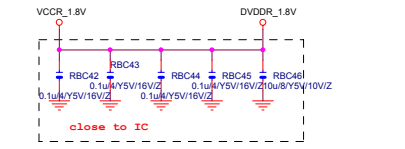
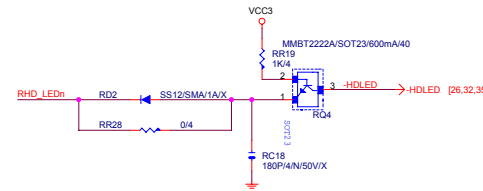
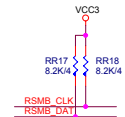
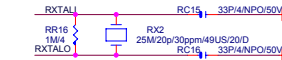
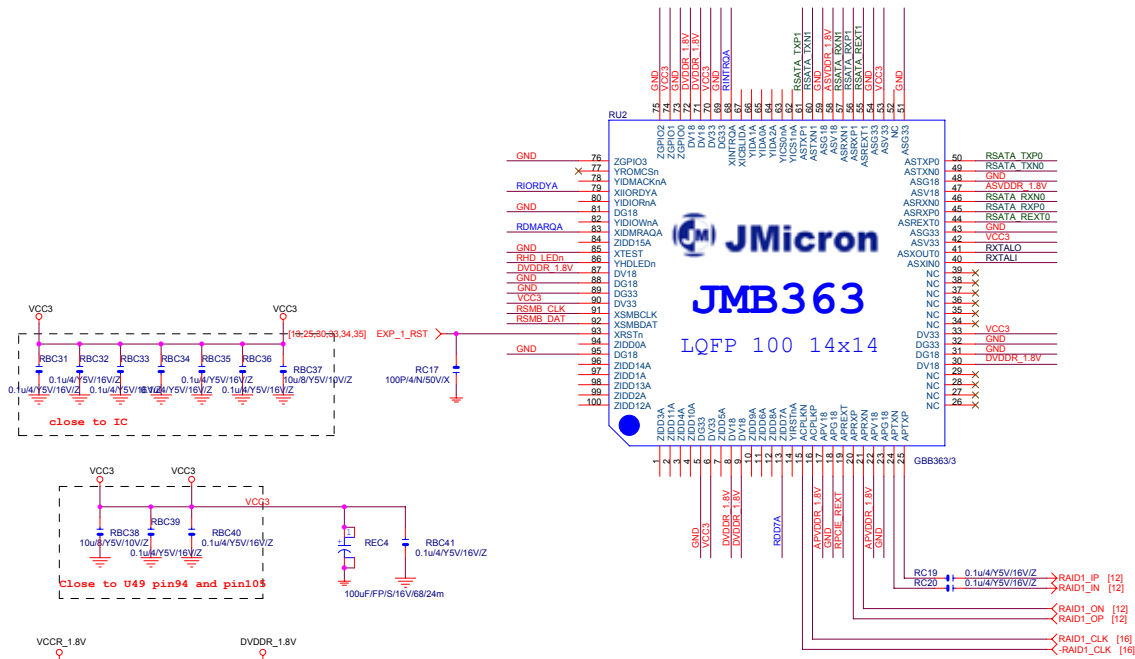


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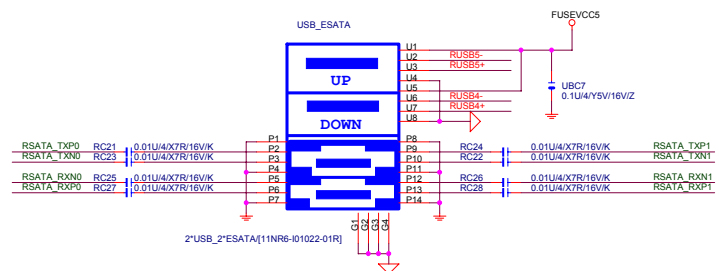
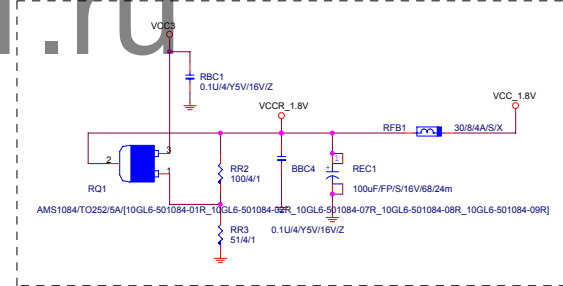




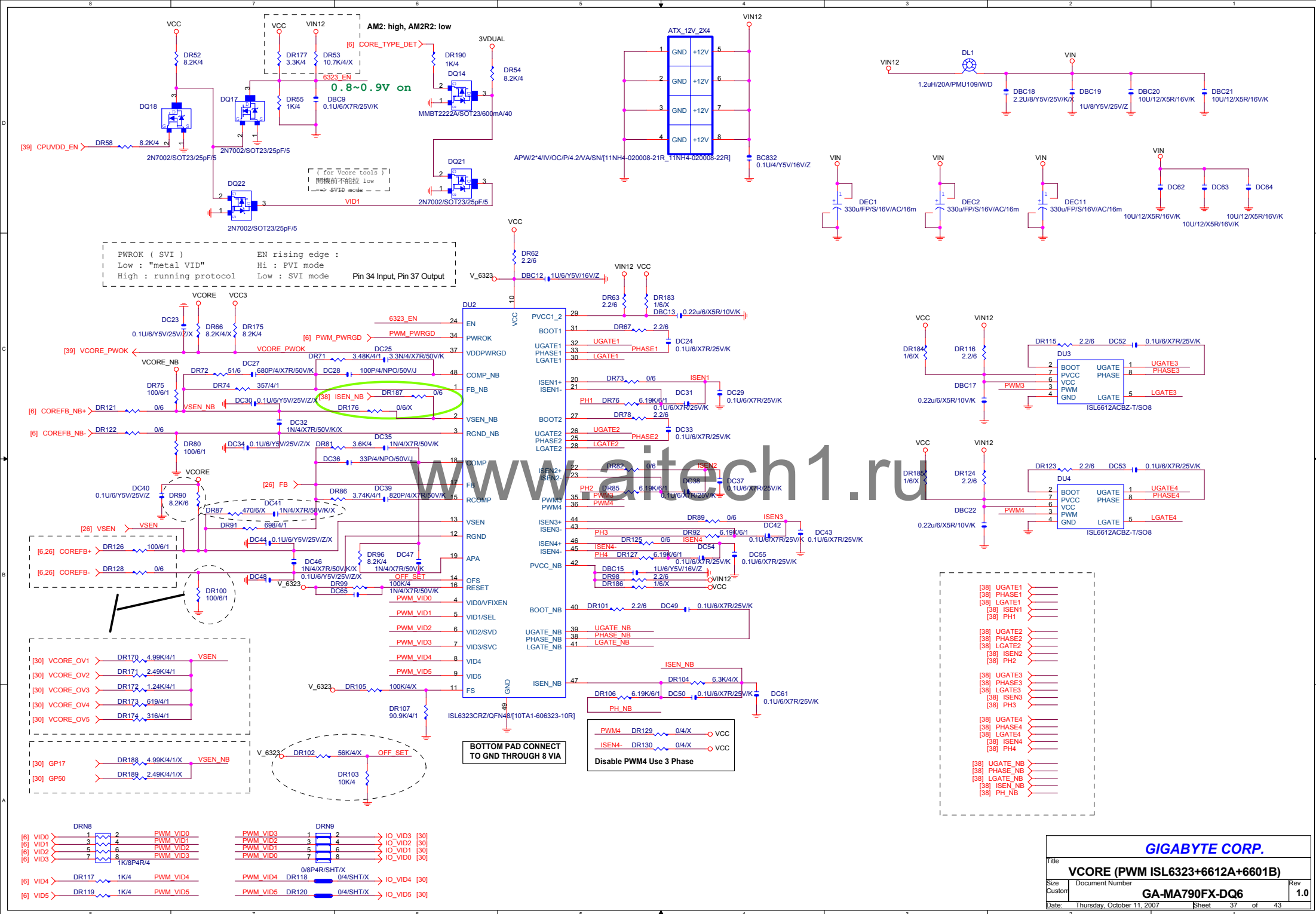


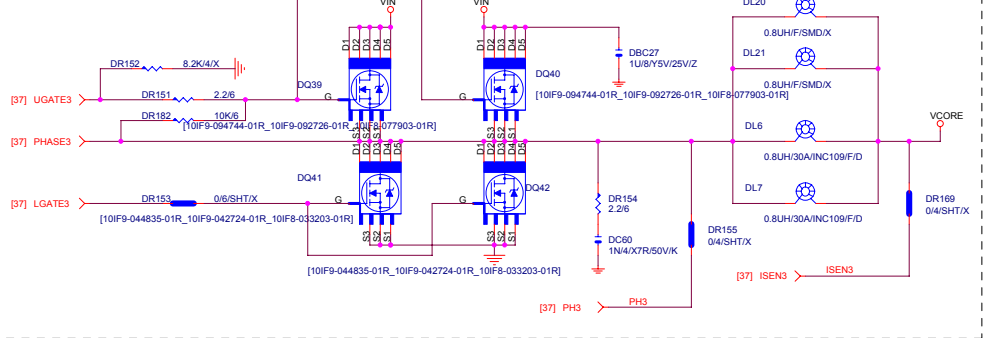
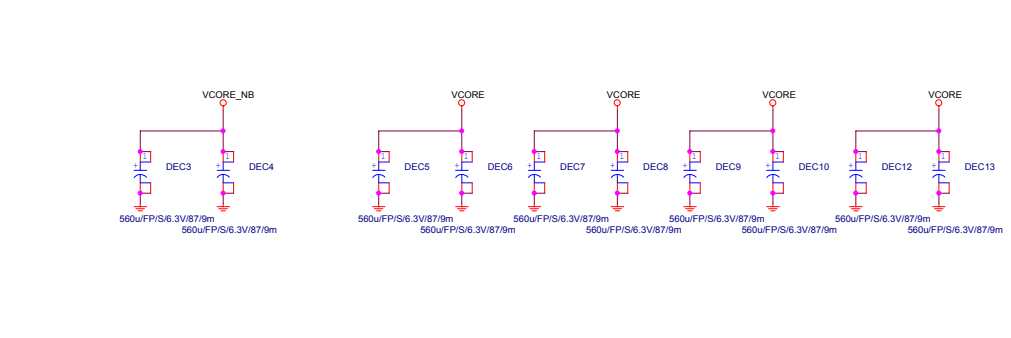
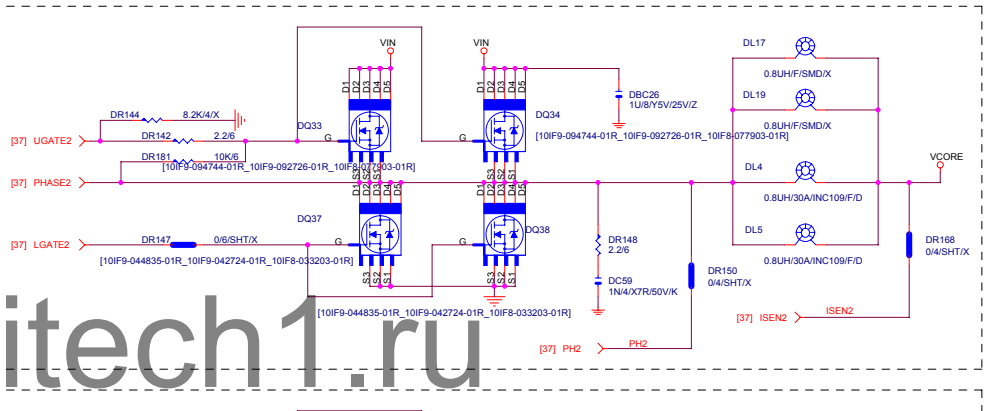
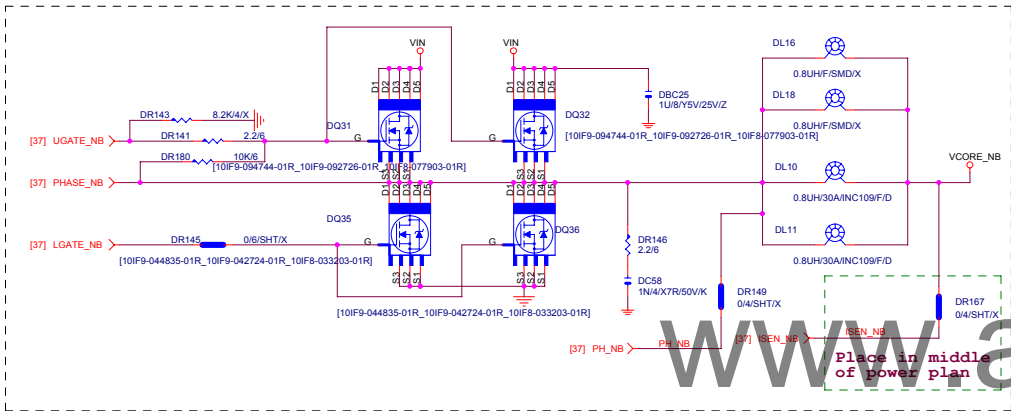
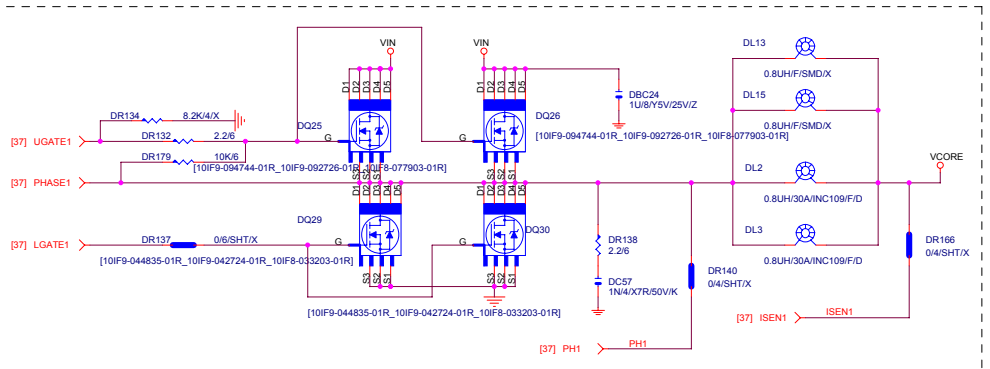
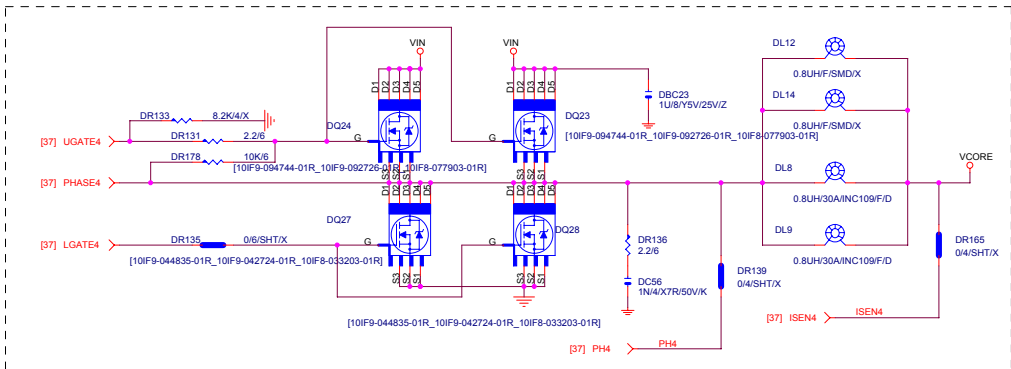


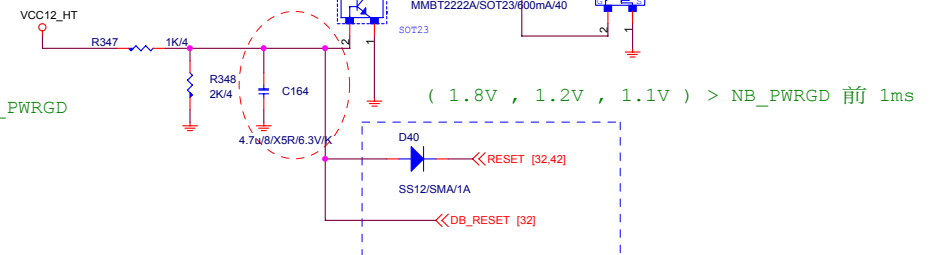
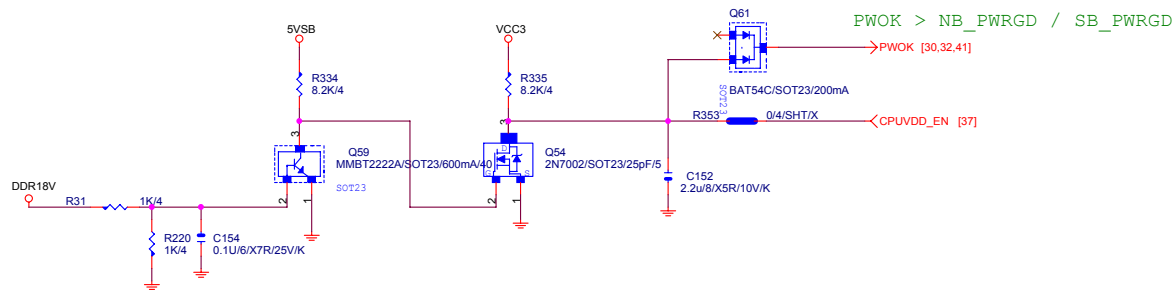
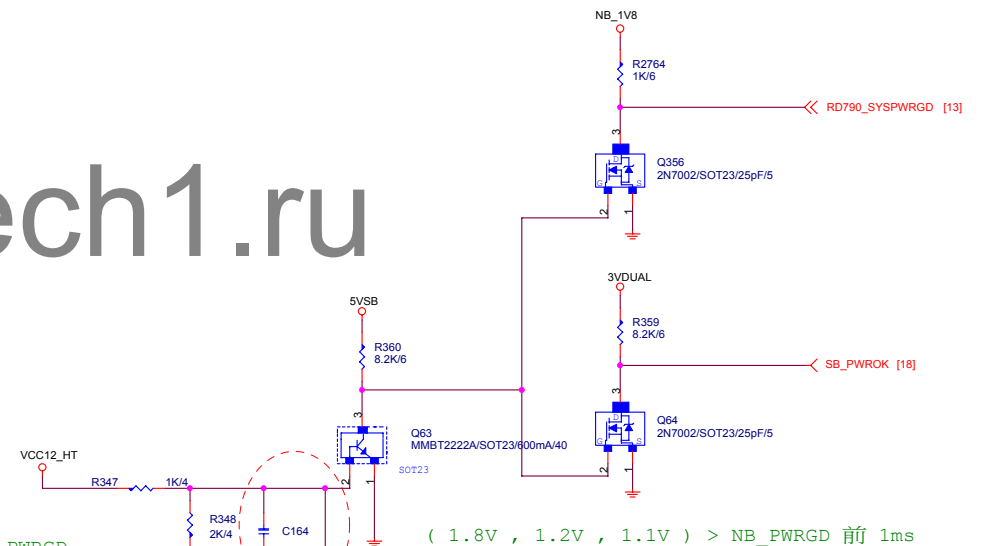
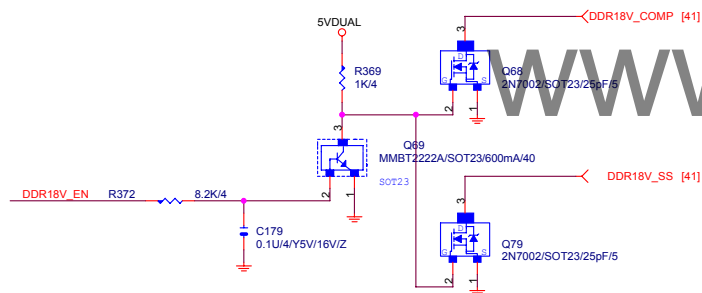
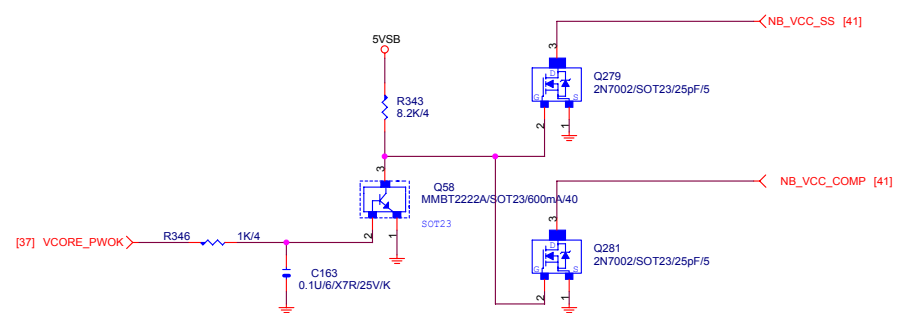
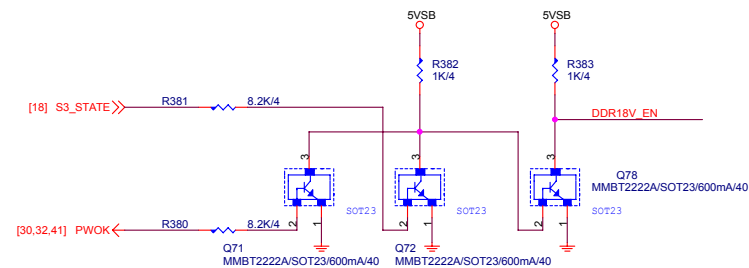
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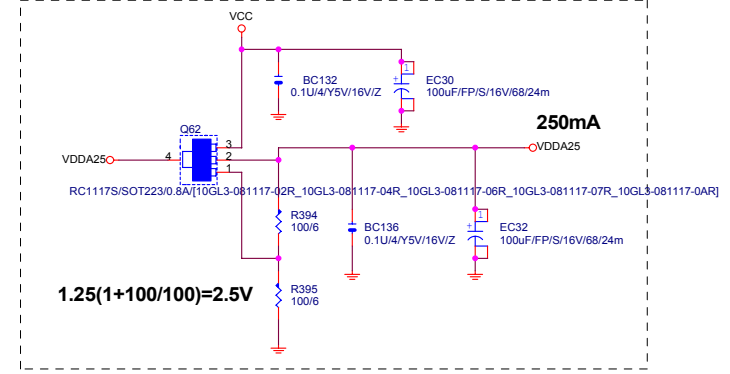
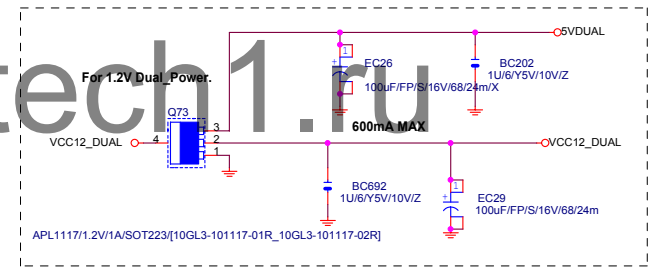
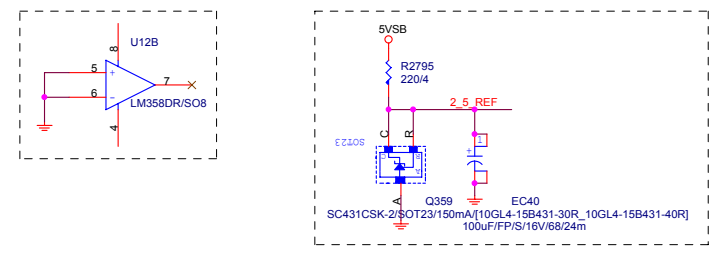
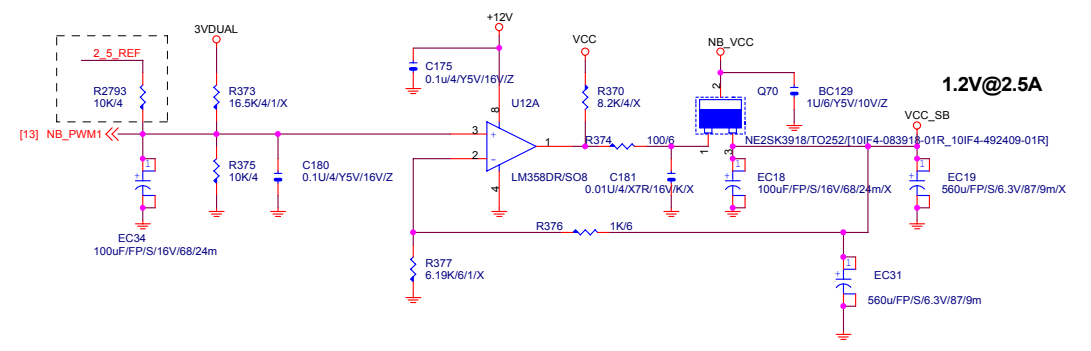
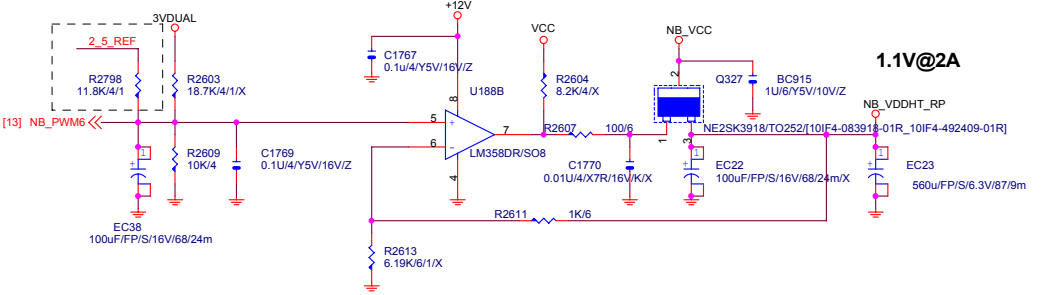
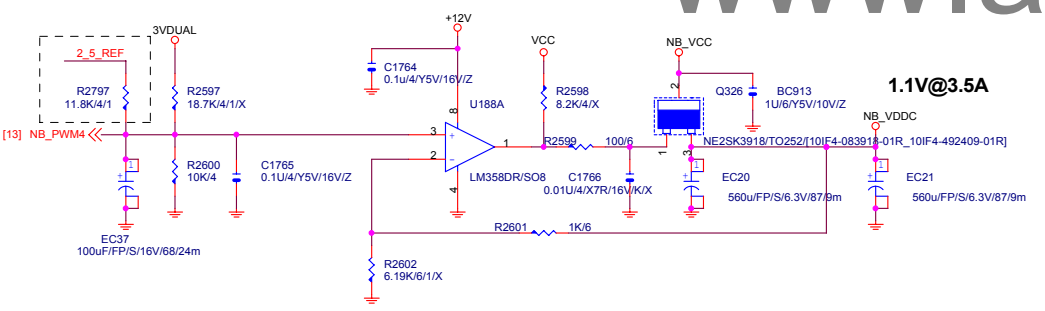
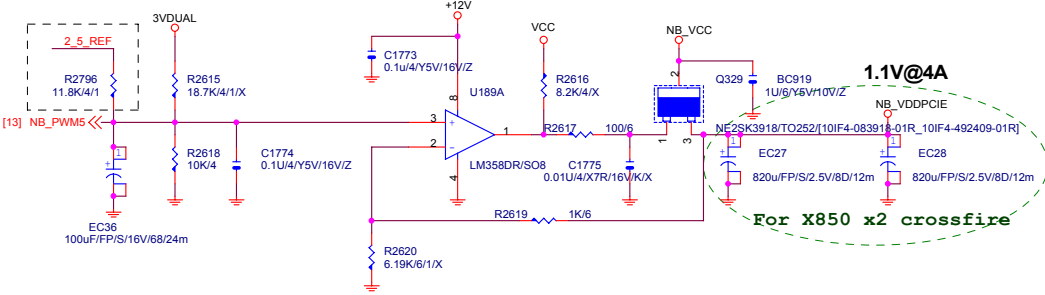
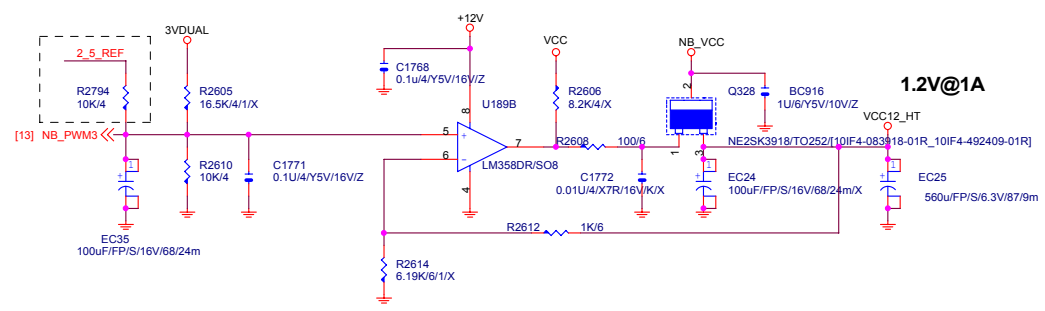








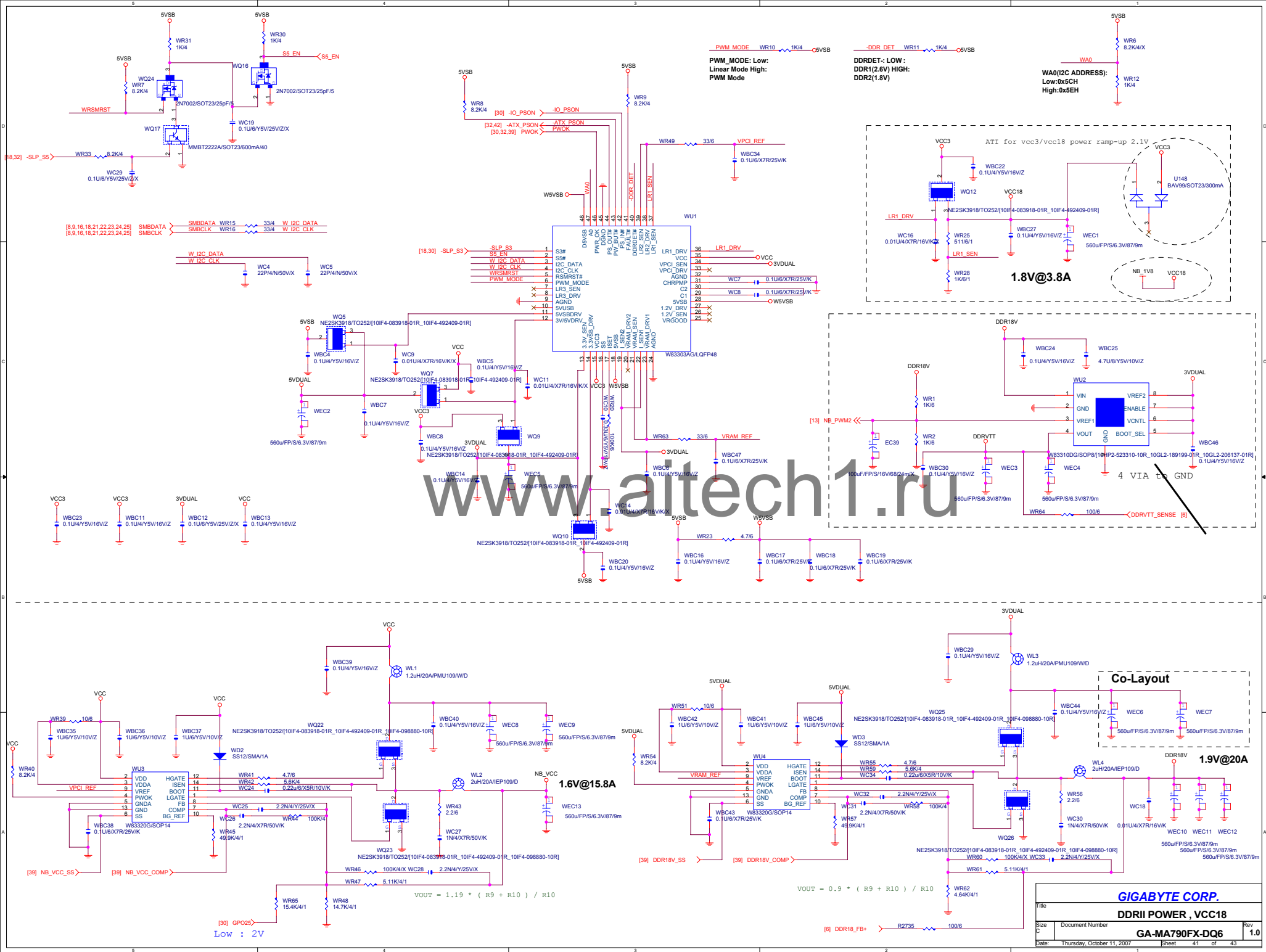
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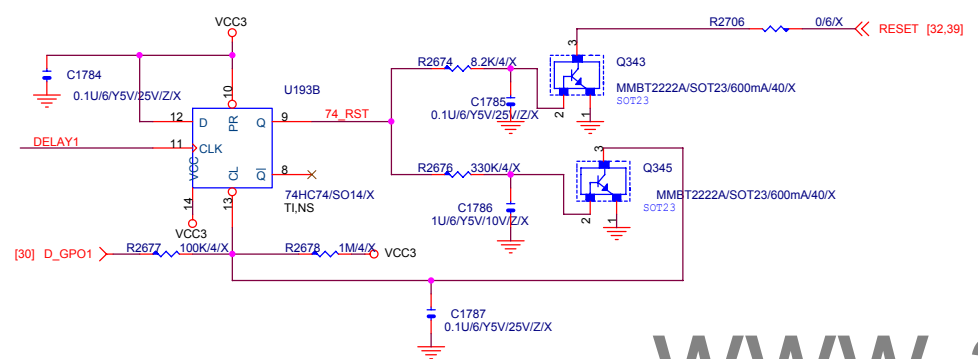
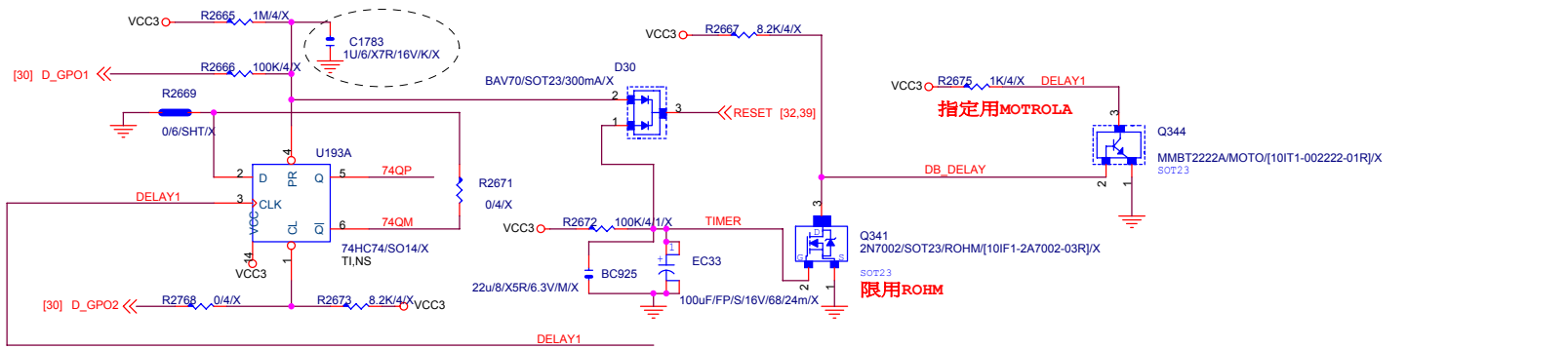


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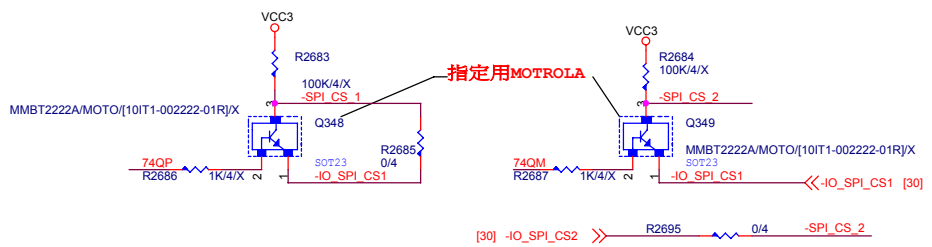
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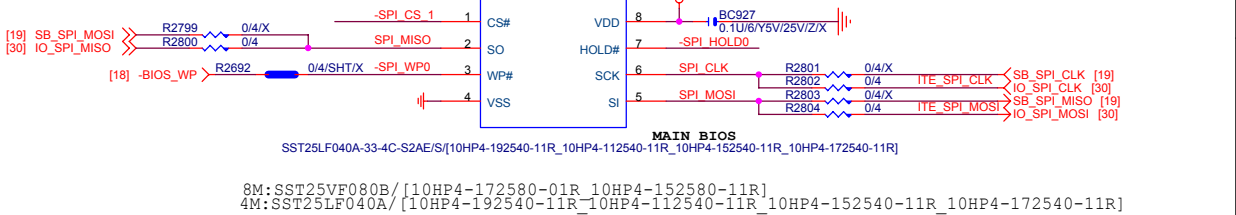
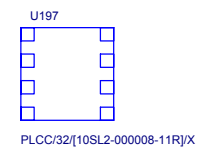
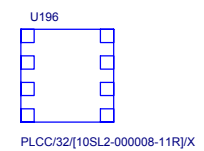




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[18] SB\_GPI04 << 74QP  
[30] D\_GPO1 >> D\_GPO1  
[30] D\_GPO2 >> D\_GPO2



-SPI\_HOLD0 R2688 8.2K/4  
-SPI\_MISO R2690 8.2K/4/X  
-SPI\_WP0 R2691 8.2K/4/X  
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靠近U24 BC926 33P/4/N/50V/X

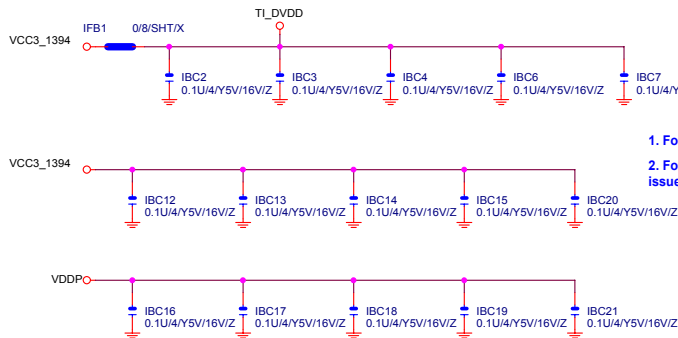
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DUAL BIOS

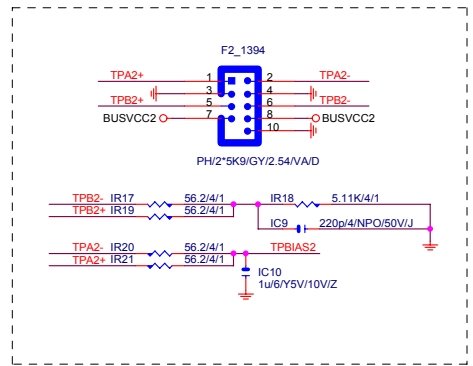
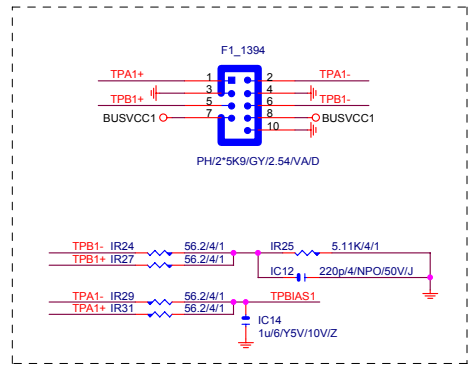
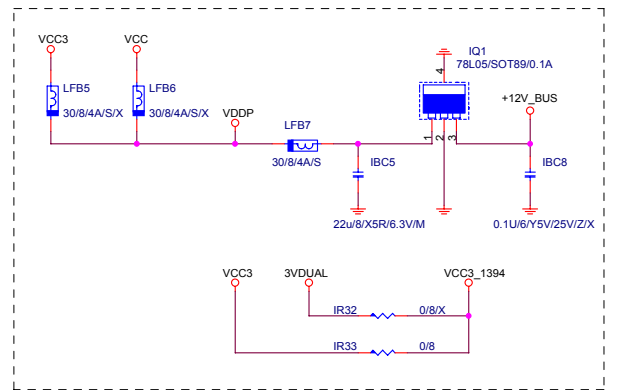
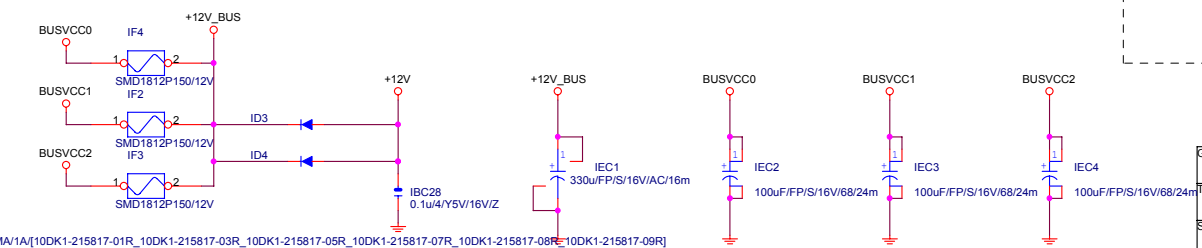
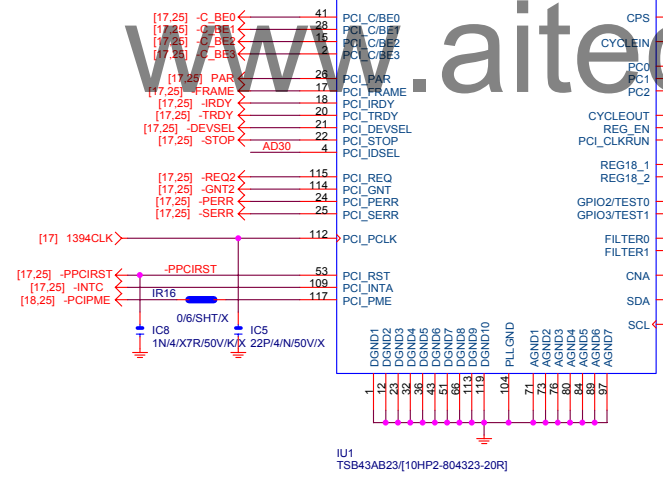
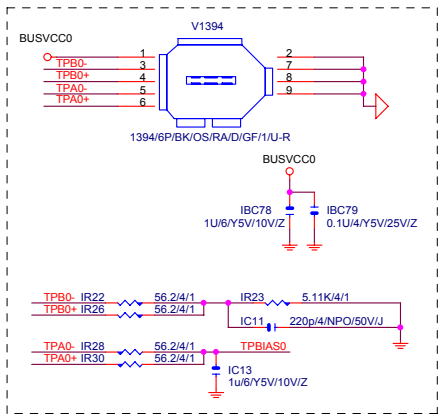
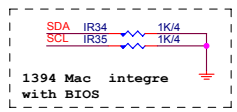
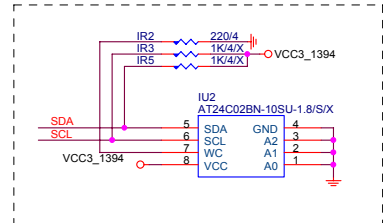
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1. For chip burn issue-->Elvis  
2. For factory M/P bear card issue, change back.



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